



A Cooperation Agreement for 10 Gigabit Ethernet Transceiver Package

Issue 2.0

26 Sept 2001

1 Revision

| Rev | Date | By | Purpose/Changes |
|-----|-------------------|----------------|---|
| 1.0 | 1 May 2001 | Antony Spilman | First Public Issue |
| 2.0 | 26 September 2001 | Antony Spilman | Finalize: mechanical dimensions, key functionality, electrical pin-outs, optical Interfaces |
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Rev2.0 Main changes

- General mechanical and dimension changes.
- Changed Fig 3 to reflect fixed orientation of Tx and Rx.
- Added OUI, LASI, and Adaptable Power proposals.
- Significant NVRAM updates.
- Clarified connector tolerancing.
- Added section 18.4 to clarify Optical Interface requirements for module interoperability.
- Deleted over-temp.
- Added idle patterns generation requirement to thermal evaluation conditions.
- Changed Test fixture to remove copper content between datum B and datum F.
- Added LSS registers.

2 Summary of MSA Group Members

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3 Summary of MSA Group Sponsors

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7 Purpose of the MSA

7.1 The contributing companies desire to establish internationally compatible sources of pluggable fiber optic transceiver modules in support of all approved implementations of the IEEE 802.3ae standard for 10 Gigabit Ethernet.

7.2 Each party desires to establish uniformity in the areas described in the section "Scope of this MSA" and detailed in the Appendix of this MSA.

7.3 Each party expects that the establishment of multiple compatible sources of front panel pluggable 10 Gigabit Ethernet modules will allow the entire fiber optic marketplace to grow more rapidly. This enhanced marketplace growth, customer choice, and vigorous competition is the express purposes of this Agreement.

8 Contribution to and distribution of this MSA.

8.1 The charter members of this MSA are Agilent Technologies, Agere Systems, Tyco Electronics, Pine Photonics Communications, Mitsubishi Electronics, Optillion, and TBA.

8.2 The final MSA document shall be made available to all Participating Members and to non-participants who request a copy, after the document is signed and complete.

9 Scope of this MSA.

9.1 The parties agree to cooperate by supporting common product specifications for pluggable fiber optic transceivers with the package "Package Dimensions", "Rail System", "Host Board Layout", "Electrical Interfaces – including Control, Monitoring and Management", and "Front Panel Bezel Requirements" as shown in the Appendix of this MSA. The overall package dimensions shall conform to the indicated dimensions and tolerances, and the mounting features shall be located such that the products are mechanically interchangeable with the rail and connector system. In addition the overall dimensions and mounting requirements for the rail and connector system on a circuit board shall be configured such that the products are mechanically and electrically interchangeable.

9.2 Each party acknowledges this agreement provides a common solution for all approved PMDs in the IEEE 802.3ae specification but may not provide an optimum solution for applications with different constraints.

9.3 The electrical and optical specifications shall be compatible with those enumerated in the appropriate standards (i.e. the IEEE 802.3ae 10 Gigabit Ethernet standard). Recommended circuit layouts for electrical input and output terminations, and grounding practices are also described in the Appendix of this MSA.

9.4 The specific PMD implementation and internal design of the module is entirely at the discretion of each party and is not covered by this Agreement. The parties recognize that their products may not be identical, but need only meet the criteria shown in the Appendix of this MSA to assure interchangeability.

9.5 This agreement relates to transceivers with transmission rates up to 10.7 Gb/s, operating over multimode and singlemode fiber.

10 Licensing and Fees relating to this MSA:

10.1 No license is granted under the patents, know-how, tradeseecrets or any other technology of any party to this Agreement either expressly or by implication or by estoppel.

10.2 Each of the MSA parties have agreed that licenses to all intellectual property necessary to realize a module conforming to this MSA will be made available to all interested parties. These licenses will be granted under reasonable and non-discriminatory terms and conditions applicable to that MSA party, conditional on the interested party also agreeing to license any necessary intellectual property to the parties of this MSA.

10.3 Individual parties to this Agreement may have patents, which they believe may be relevant to this Agreement. The MSA parties should be contacted individually to determine if they have patent rights, which they believe may be pertinent to this Agreement. Each party is free to seek technology or other exchanges with other firms in order to support its activities under this Agreement.

10.4 Each party agrees to be responsible for its own development, manufacturing, marketing and selling in order to supply transceivers meeting the attached specifications.

10.5 This Agreement does not preclude any party from offering other products that may not meet the attached specifications.

10.6 Each party retains complete liberty regarding its methods of implementing a supply of product, e.g., by engineering effort or by technology licensing or transfer or combination of these or other practices.

10.7 Each party also retains sole discretion in its choice of sales channels and distribution.

10.8 Each party affirms its intention to compete freely and openly in the marketplace with the parties as well as other competitors. Each party expects to support products meeting the attached specifications for as long as marketplace conditions warrant. No specific time limit is associated with this Agreement. The determination of market condition suitability is to be made by each party individually and in each party's sole discretion.

11 Operating Guidelines

11.1 Any new action item, design change, membership action, decision on public information disclosure, or other activity related to this MSA or its Guidelines will require the approval of a minimum of 75% of the MSA group. Members abstaining from voting are not to be considered in this percentage. No response will be interpreted as agreement to the proposed change. Each participating company will have one vote.

11.2 Each Participating Company must identify the person(s) in their organization that have the authority and responsibility to sign the final MSA. At least one such person, or delegate with full authority to represent the Company, must participate in each meeting and will have the single vote for that Company. If a Company fails to attend a MSA meeting twice in succession, they will be subject to a vote of removal from the MSA.

11.3 If a non-represented Optical Transceiver Company asks to join the MSA, they may join the discussions if they are willing to agree to the operating guidelines and accept the current MSA specifications in their entirety. New members will not be allowed to revisit work already established, or to make motions or vote to change existing designs, parameters, or characteristics. Additionally, approval of at least 75% of the current members will be required to admit new members.

11.4 There will be no permanent Chairperson for this group, though the position can be created by approval of at least 75% of the members.

11.5 Each Participating Company's representatives will treat the Substance of the MSA Discussions as confidential until such time as it is agreed by the participants to make a simultaneous Public disclosure. If the participant group agrees to discuss specific MSA details with the market before making a decision, this may be done with a 75% majority vote. It is acceptable to tell the market that discussions to achieve an MSA are underway without mentioning timing, content, number or names of participants, or possible outcomes of the discussions.

11.6 Companies may be removed from the MSA group by vote of a minimum of 75% of the group. Members abstaining from voting are not to be considered in this percentage. The vote will decide whether loss of voting rights or removal from the group will be imposed.

12 Sponsoring Members

12.1 Sponsoring Members (Sponsors) will be equipment manufacturers or service providers in the networking communications industry.

12.2 Sponsors will be recruited to provide design input and validation of the work created by the MSA.

12.3 Sponsors will:

- Have full access to all specifications of this MSA and meeting minutes.
- Be admitted to all meetings or teleconferences called by the MSA group. Such admission will be limited to 1 representative per company to allow for manageable and focussed meetings.
- Will be encouraged to provide recommendations to add features or functions, to clarify the operation of devices described by this document, or to otherwise suggest modifications this document.
- Not participate in voting to modify this MSA or its Guidelines.
- be admitted or removed from the MSA by action of the Group.

13 Announcing and Promoting the Agreement

13.1 This MSA and the form factor that it describes will be known as the “XENPAK”. Examples of how this term would be used include (but are not limited to):

The “XENPAK MSA group”

The “XENPAK form factor”

It will not be acceptable to use the shortened term, “XEN”.

13.2 Each party agrees to announce this Agreement in a manner agreed upon by the parties, such announcements will mention all the parties who have signed this Agreement.

13.3 Each party agrees to seek public attention by means of such an announcement.

13.4 Each party agrees to use the XENPAK name in reference to this MSA in announcements and promotional efforts.

13.5 Each party agrees to use any “image” guidelines agreed by the group when referring to the XENPAK MSA such as logo’s or other identity elements that have been defined by the group.

13.6 After the Agreement is announced, each party may advertise or otherwise promote this Agreement in any way that it deems appropriate. Other parties to this agreement can be mentioned by name when used to discuss the activities of this group without the other party’s prior consent.

14 Other Vendors

14.1 The parties recognize that additional vendors may choose to match the attached product specifications after this Agreement is announced.

14.2 Each party recognizes it is desirable and keeping with the intent of the Agreement for such additional vendors to support the transceiver mechanical dimensions and functional attributes described in the Appendix of this MSA. Therefore, each party agrees to encourage other vendors to support these product specifications, after this Agreement is announced.

15 Future Direction

15.1 *Current Product:* Should the parties agree to further explore technical and other exchanges pertaining to the products described in this Agreement, then this shall be under a separate agreement.

15.2 *Withdrawal:* The parties recognize that at some future time it may become less feasible to offer the products envisioned by this Agreement. A party may withdraw from its commitment to cooperate at its own discretion upon a 90-day notice to the other parties.

16 Limitation of Liability

16.1 With the exception of disputes arising out of intellectual property issues, no party to this Agreement shall be liable for any indirect, incidental, punitive, or consequential damages, including without limitation, lost profits or changes of good will, or similar losses, even if advised of the possibility of such damages. In addition, each party's liability under this Agreement for direct damages shall be limited to \$10,000.

17 Membership sign up form

On behalf of [Company Name]:

Address:

Membership Category:
(Check One).

Normal

Sponsor

We agree to the terms and conditions of the XENPAK MSA guidelines as described in section seven (7) through sixteen (16), and request membership to the MSA group.

by:

Signed

Name

Title

Date

18 MSA Mechanical

Fig 1. Isometric Drawings

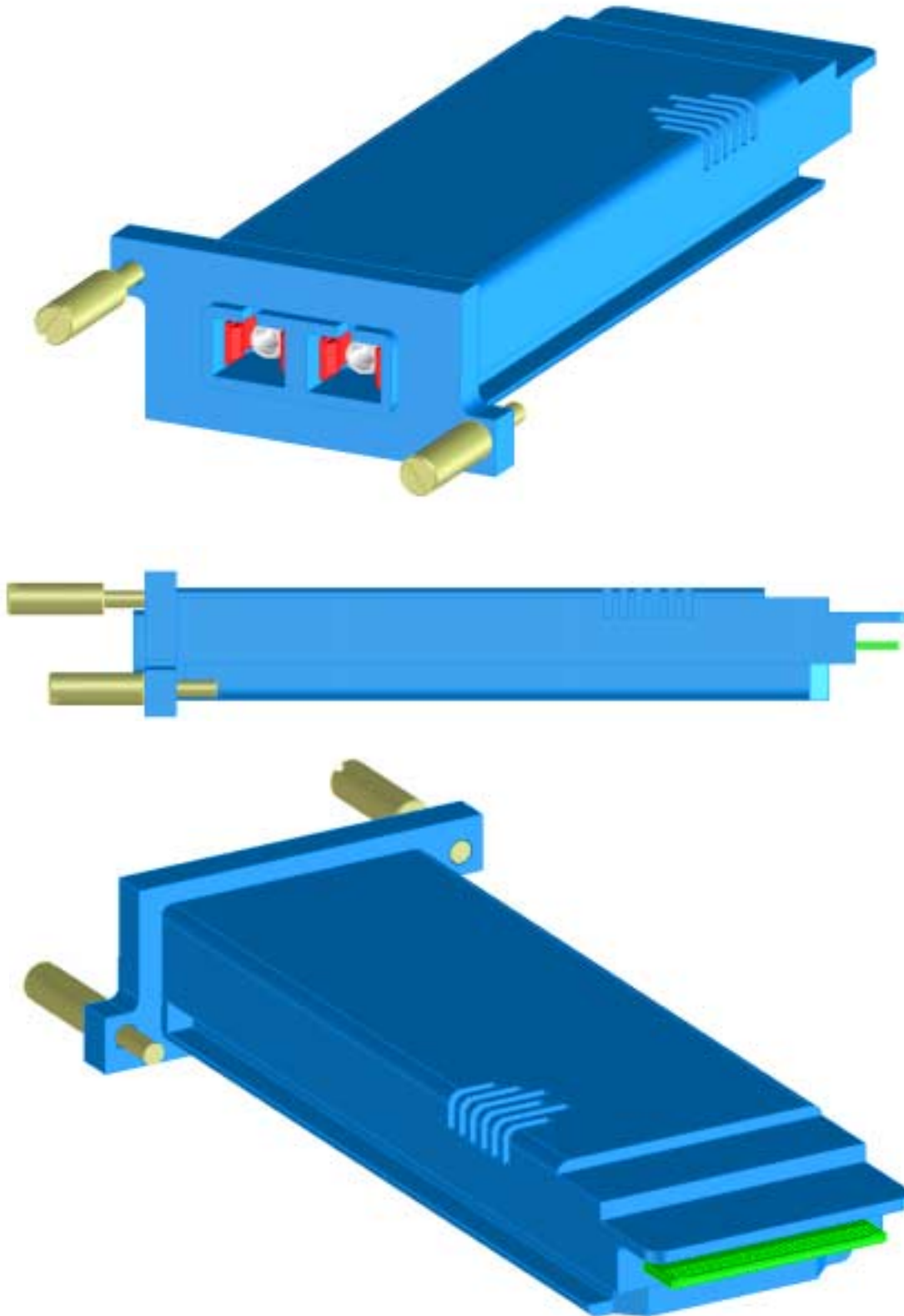
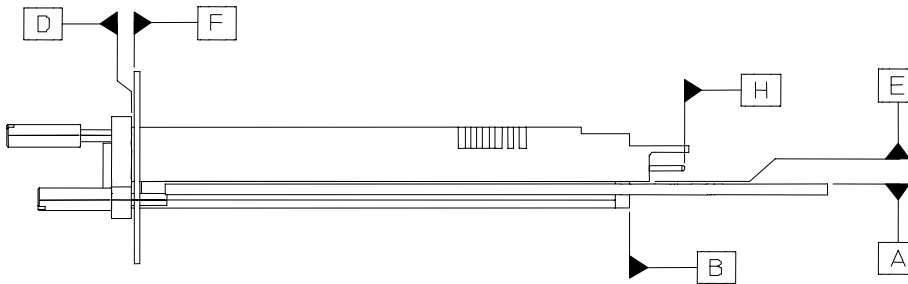
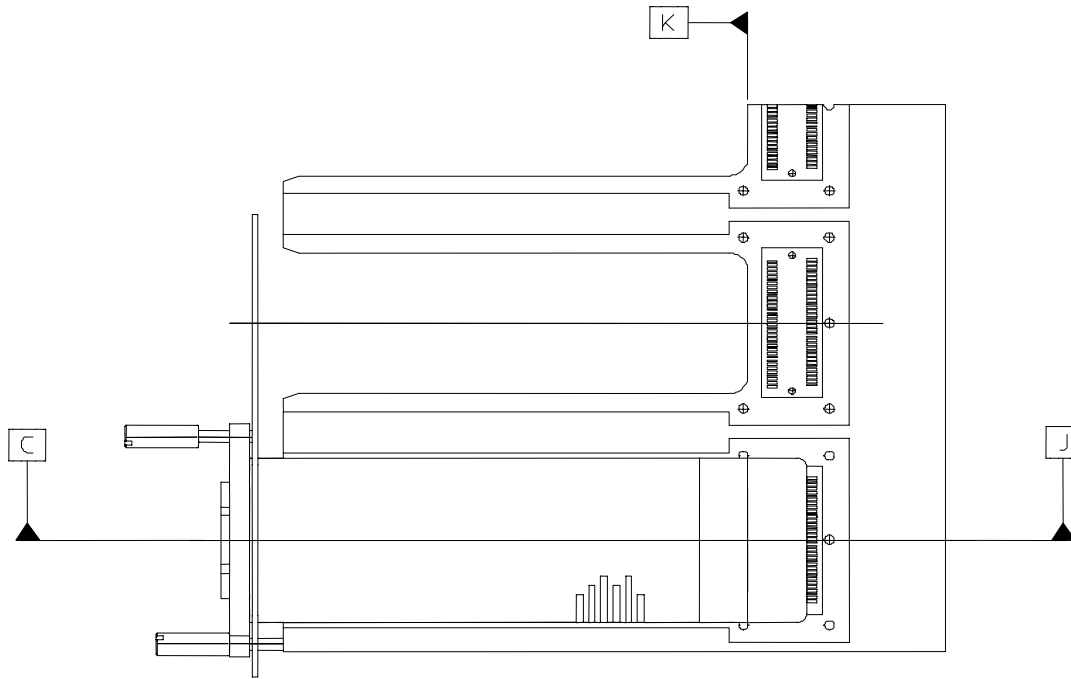


Fig 2. DATUM Legend figure updated



Definition of Datums

| DATUM | DESCRIPTION TRANSCEIVER / LINECARD |
|-------|---|
| A | CUSTOMERS PCB TOP SURFACE |
| B | PHYSICAL HARD STOP FOR TRANSCEIVER TO CUSTOMERS PCB |
| C | CENTER VERTICAL PLANE OF TRANSCEIVER |
| D | BACK SURFACE OF TRANSCEIVER BEZEL, SAFETY HARD STOP |
| E | TRANSCEIVER TOP SURFACE OF SLOT 'P1' |
| F | FRONT SURFACE OF CUSTOMERS FACEPLATE |
| G | WIDTH OF TRANSCEIVERS PCB, SEE FIG 6 |
| H | LEADING EDGE OF TRANSCEIVER PCB |
| J | CENTER VERTICAL PLANE OF CUT-OUT IN CUSTOMERS PCB |
| K | PHYSICAL HARD STOP ON CUSTOMERS PCB |

Fig 3. ORIENTATION KEYING OF TX AND RX ORIENTATION Vs PCB

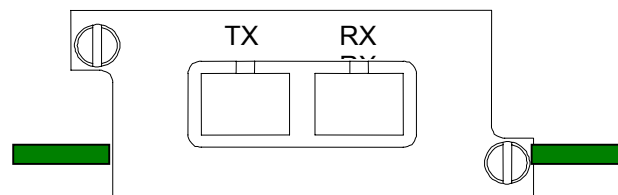
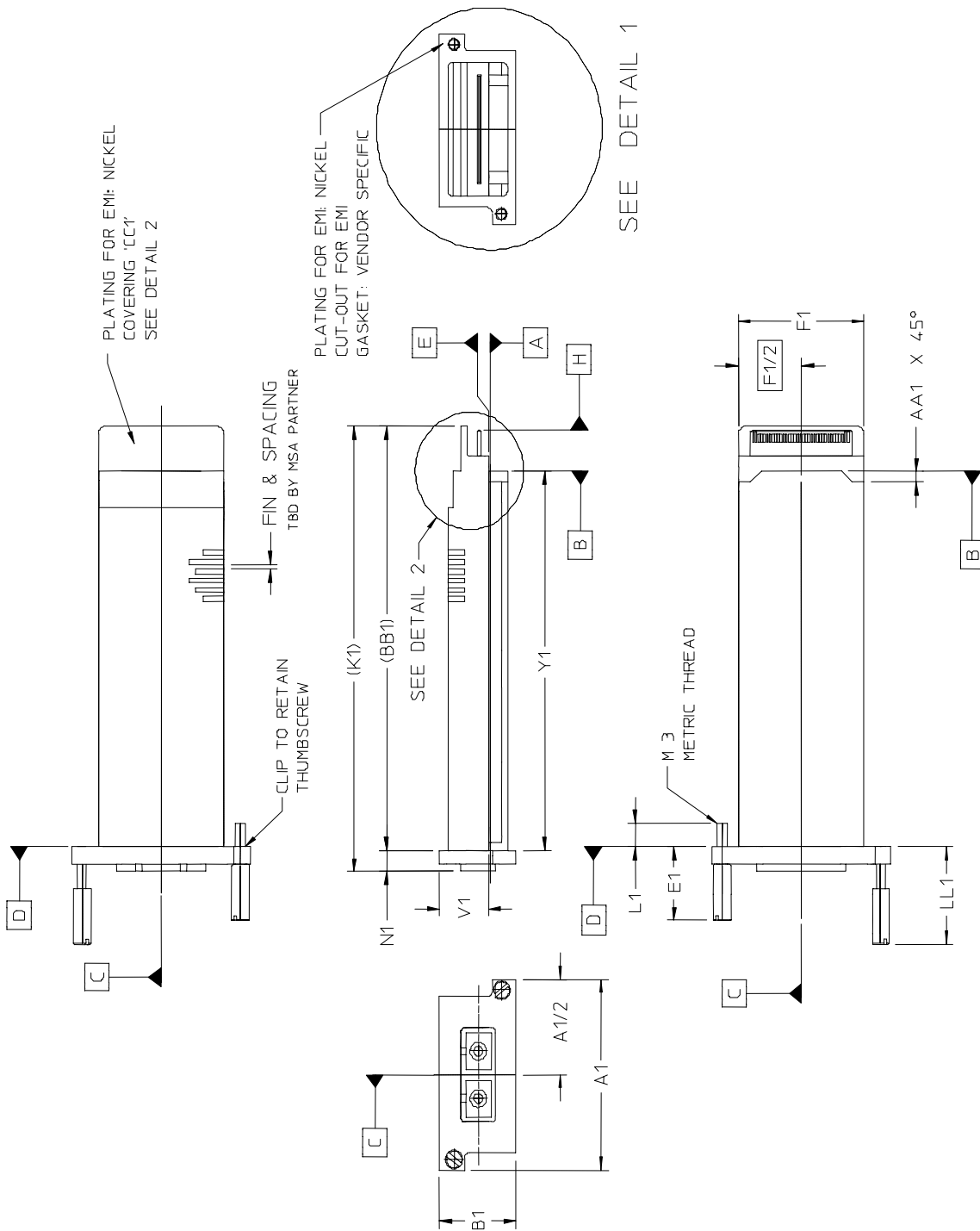


Fig 4. Package Outline

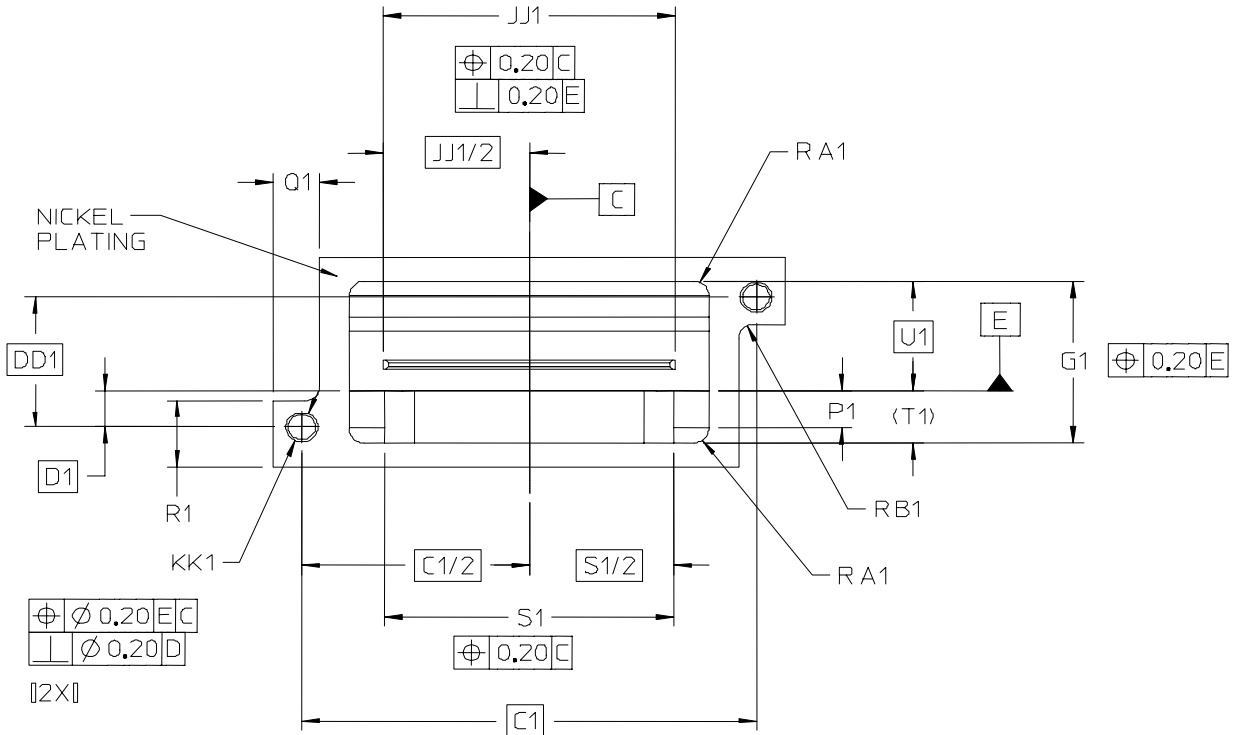
Refer to Table 1 for Dimensions



NOTE:
The SC Duplex Receptacle shall conform to the requirements of IEC 61754-4 with the following clarification:
The distance between the center line of the active optical bores (ref DB) shall be 12.25/13.15mm to match the floating duplex SC optical plug (ref Duplex optical plug table Note 8).

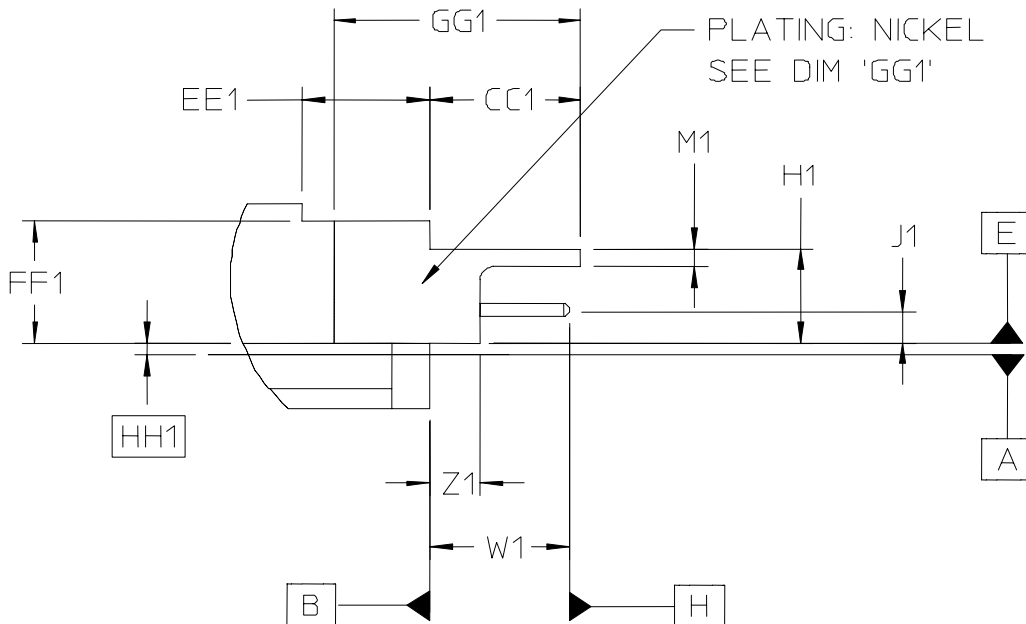
Package Outline (cont'd)

Refer to Table 1 for Dimensions



DETAIL 1
SCALE 2X

END VIEW OF TRANSCEIVER



SIDE ELEVATION TRANSCEIVER

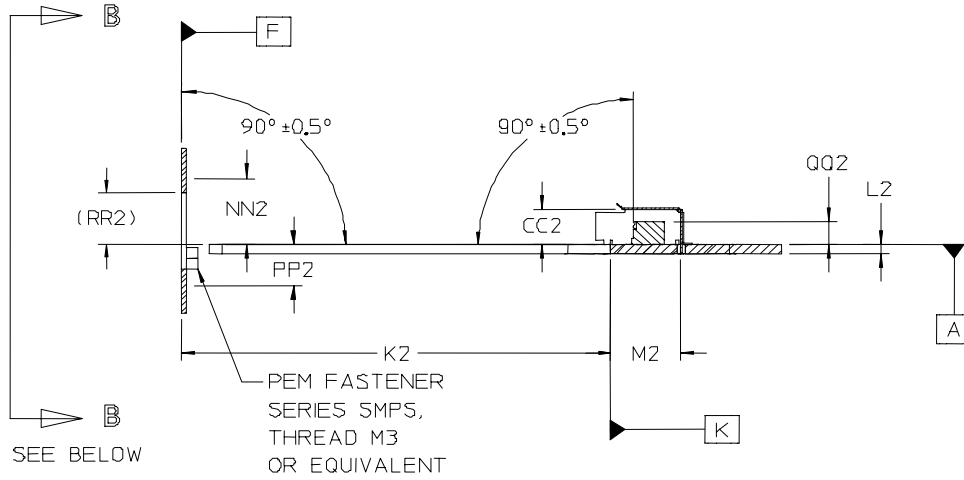
DETAIL 2
SCALE 2X

Table 1 Package Dimensions

| KEY | VALUE, mm (inch) | | TOLERANCE mm | COMMENTS |
|------|------------------|-----------------|-----------------|--|
| A1 | 51.3 | (2.019) | ± 0.20 | Width of Bezel overall |
| B1 | 24.4 | (0.961) | ± 0.20 | Height of Bezel overall |
| C1 | 45.5 | (1.791) | BASIC | Distance between captive screws in 'X' axis (Horizontal) |
| D1 | 3.95 | (0.156) | BASIC | Datum 'E' to lower captive screw |
| E1 | 20.75 | (0.817) | MAX | Extension of captive screw |
| F1 | 36.0 | (1.417) | ± 0.10 | Width of Transceiver body |
| G1 | 17.4 | (0.685) | ± 0.10 | Height of Transceiver body |
| H1 | 7.90 | (0.311) | ± 0.10 | Datum 'E' to top of Over-hanging Ledge |
| J1 | 2.80 | (0.110) | ± 0.10 | Datum 'E' to centerline of Transceiver PCB |
| K1 | 121.0 | (4.76) | REF | Length of Transceiver overall minus protruding captive screw heads |
| L1 | 5.00 | (0.24) | ± 0.20 | Length of captive screw from Datum 'D' to end of threaded end |
| M1 | 1.5 | (0.059) | ± 0.10 | Thickness of Over-hanging Ledge |
| N1 | 5.75 | (0.226) | ± 0.20 | Thickness of Transceiver Bezel |
| P1 | 2.36/3.88 | (0.093 / 0.153) | N/A | Slot to accommodate Customers PCB range. |
| Q1 | 4.65 | (0.183) | ± 0.10 | Protrusion of side flange on Transceiver Bezel |
| R1 | 8.12 | (0.320) | ± 0.10 | Height of side flange on Transceiver Bezel |
| S1 | 29.5 | (1.161) | ± 0.10 | Width of Transceiver slot to accommodate rail or Customers PCB |
| (T1) | 5.67 | (0.223) | REF | Datum 'E' to bottom of Transceiver |
| U1 | 11.73 | (0.462) | BASIC | Datum 'E' to top of Transceiver |
| V1 | 15.23 | (0.60) | ± 0.10 | Datum 'E' to top of Transceiver Bezel |
| W1 | 11.10 | (0.437) | ± 0.20 | Datum 'B' to end of protruding Transceiver PCB |
| Y1 | 102.20 | (4.020) | ± 0.20 | Datum 'D' to Datum 'B' |
| Z1 | 4.0 | (0.157) | ± 0.20 | Datum 'B' to end of side protective shroud to mate with EMI/Conn. Shield |
| AA1 | 3.0 | (0.118) | ± 0.50 | Datum 'B' to end of 45° chamfer |
| BB1 | 115.25 | (4.537) | REF | Length of Module from Datum 'D' to rear Over-hanging Ledge |
| CC1 | 13.0 | (0.512) | ± 0.50 | Datum 'B' to end of Over-hanging Ledge for Nickel Plating |
| DD1 | 13.96 | (0.550) | BASIC | Distance between captive screws in 'Y' axis (Vertical) |
| EE1 | 10.0 | (0.394) | N/A | Datum 'B' end of recess for insertion clearance |
| FF1 | 10.23 | (0.402) | ± 0.50 | Datum 'E' to top of recess for insertion clearance |
| GG1 | 20.0 | (0.787) | N/A | Length of Transceiver side wall for Nickel plating |
| HH1 | 0.50 | (0.020) | BASIC | Datum 'A' to Datum 'E' |
| JJ1 | 29.2 | (1.150) | REF | Width of Transceiver PCB |
| KK1 | 3.0 | (0.118) | N/A | Hole for Thumbscrew, tapped or clearance for 3mm screw |
| LL1 | 25.8 | (1.016) | N/A | Length of Thumbscrew in outer position |
| RA1 | 1.5 | (0.059) | N/A | Maximum external radius or chamfer of Transceiver |
| RB1 | 1.5 | (0.059) | N/A | Maximum Internal radius or chamfer on exterior of Transceiver Bezel |

Fig 5. Front Panel Opening and Host PCB

Refer to Table 2 for Dimensions



CROSS SECTION A-A
CUSTOMERS PCB AND FACEPLATE

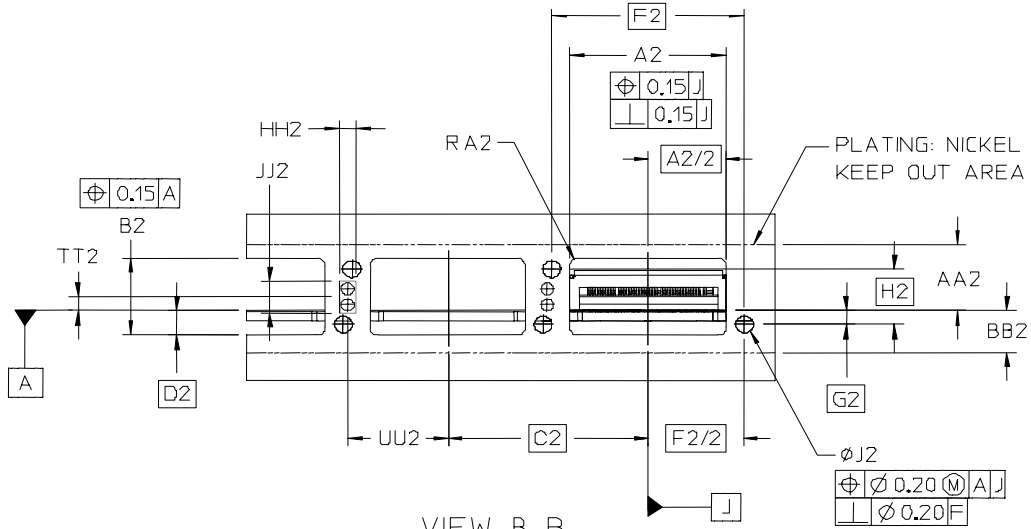
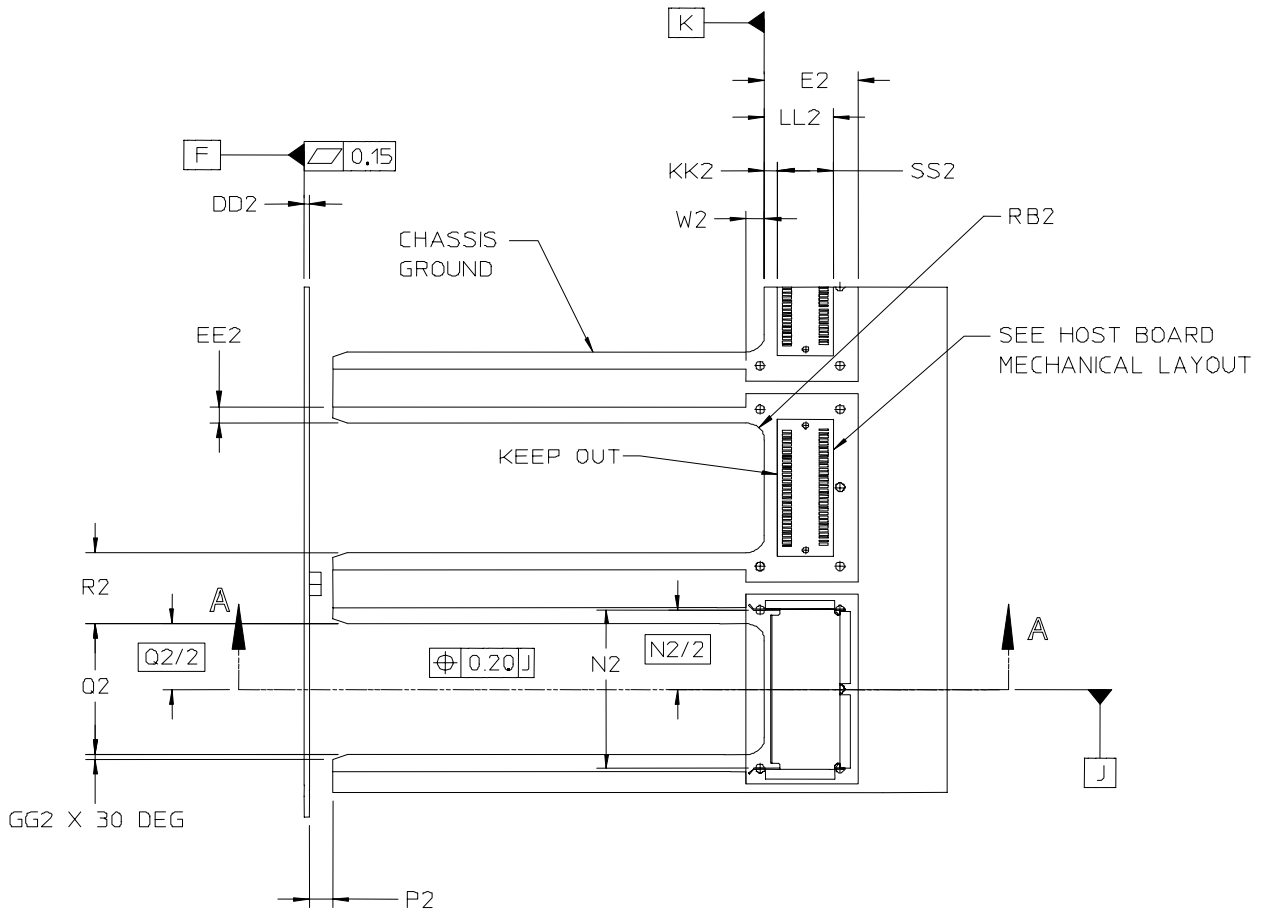


Fig 5(cont'd)

Refer to Table 2 for Dimensions



PLAN VIEW CUSTOMERS PCB

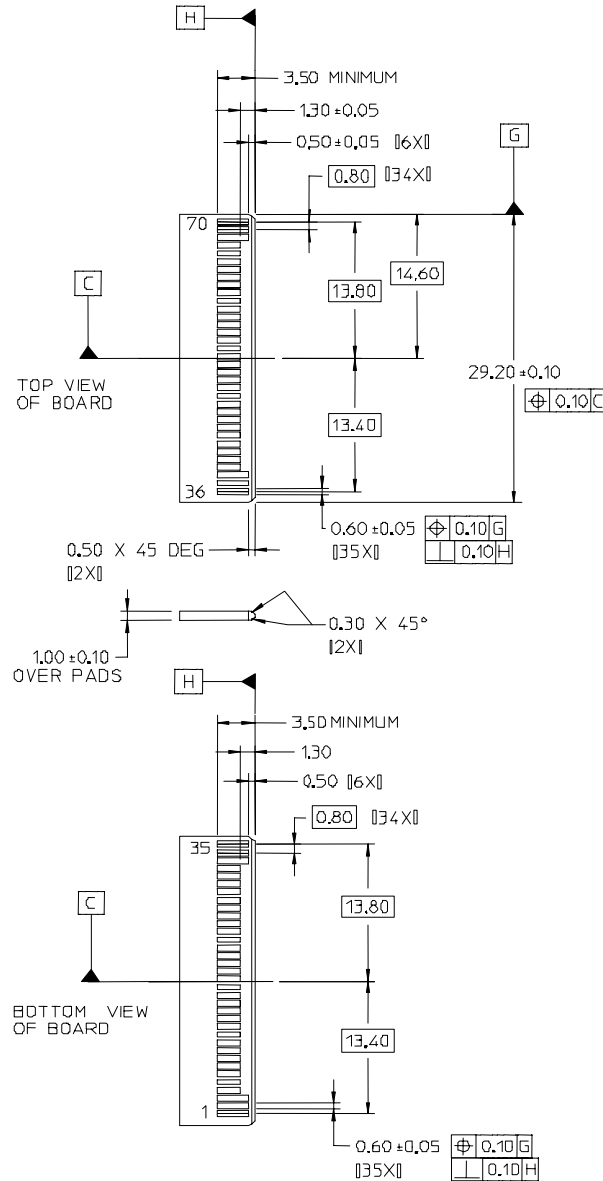
Table 2 Front Panel Opening and Host PCB Dimensions

| KEY | VALUE, mm (inch) | | TOLERANCE mm | COMMENTS |
|-----|------------------|-----------------|-----------------|--|
| A2 | 37.0 | (1.457) | ± 0.20 | Width of cut-out of Customers sheet metal Faceplate |
| B2 | 19.4 | (0.764) | ± 0.20 | Cut-out in Customers sheet metal Faceplate 'Y' axis (Vertical) |
| C2 | 47.47 | (1.869) | BASIC | Minimum Spacing of Modules |
| D2 | 6.17 | (0.243) | BASIC | Datum 'A' to bottom cut-out of the Customers sheet metal Faceplate |
| E2 | 20.59 | (0.810) | ± 0.30 | Datum 'B' far side of Chassis Ground |
| F2 | 45.50 | (1.791) | BASIC | Distance between holes for captive fastener in 'X' axis (Horizontal) |
| G2 | 3.45 | (0.136) | BASIC | Datum 'A' to lower mounting hole in Customers sheet metal Faceplate |
| H2 | 10.51 | (0.414) | BASIC | Datum 'A' to upper mounting hole in Customers sheet metal Faceplate |
| J2 | 4.24 | (0.167) | -0.0/+0.08 | Diameter of hole for Self Clinching Nut |
| K2 | 101.6 | (4.000) | ± 0.50 | Datum 'B' to front of Customers sheet metal Faceplate Datum 'F' |
| L2 | 2.36 / 3.88 | (0.093 / 0.153) | N/A | Customers PCB thickness range |
| M2 | 16.47 | (0.648) | ± 0.20 | Datum 'B' to back inside surface of Connector/EMI shield |
| N2 | 37.00 | (1.457) | ± 0.20 | Width of inside surface of Connector/EMI Shield |
| P2 | 6.35 | (0.250) | ± 0.50 | Distance from edge of customers PCB to inside surface of Customers S/M Faceplate |
| Q2 | 30.5 | (1.200) | ± 0.20 | Width of Cut-out in Customers PCB |
| R2 | 16.72 | (0.658) | NA | Minimum width of support on Customers PCB |
| S2 | 18.62 | (0.733) | BASIC | Datum 'J' to EMI shield mounting hole |
| T2 | 2.00 | (0.079) | ± 0.10 | EMI Shield mounting hole on Customers PCB |
| U2 | 0.98 | (0.039) | BASIC | Datum 'B' to EMI Shield mounting hole |
| V2 | 9.00 | (0.354) | BASIC | Datum 'B' to Connector mounting hole |
| W2 | 4.00 | (0.157) | ± 0.20 | Datum 'B' to front keep-out pad for EMI Shield |
| X2 | 16.59 | (0.653) | BASIC | Datum 'B' to EMI Shield mounting hole |
| Y2 | 22.30 | (0.878) | ± 0.20 | Datum 'J' to side keep-out pad for EMI Shield |
| AA2 | 16.0 | (0.63) | Minimum | Datum 'A' to upper Keep-out on Customers sheet metal Faceplate |
| BB2 | 9.0 | (0.35) | Minimum | Datum 'A' to lower Keep-out on Customers sheet metal Faceplate |
| CC2 | 8.90 | (0.350) | ± 0.20 | Datum 'A' to EMI Shield inside surface |
| DD2 | 0.63 / 2.00 | (0.025 / 0.080) | ± 0.10 | Thickness of Customers sheet metal Faceplate |
| EE2 | 4.00 | (0.157) | N/A | Minimum width for Transceiver Grounding, Proposed: Immersion gold on Nickel |
| FF2 | 1.55 | (0.061) | ± 0.05 | Hole Diameter for mounting Connector |
| GG2 | 1.20 | (0.047) | ± 0.20 | Lead in Chamfer on Customers PCB |
| HH2 | 4.00 | (0.157) | ± 0.30 | Width of reserved space for LED bank |
| JJ2 | 8.00 | (0.315) | ± 0.30 | Height of reserved space for LED bank |
| KK2 | 2.90 | (0.114) | ± 0.30 | Datum 'B' to front of reserved space for Connector Pads |
| LL2 | 15.00 | (0.590) | ± 0.30 | Datum 'B' to back of reserved space for Connector Pads |
| MM2 | 16.30 | (0.642) | ± 0.30 | Datum 'J' to side of reserved space for Connector Pads |
| NN2 | 13.8 | (0.543) | Minimum | Datum 'A' to minimum Flat area on Customer Faceplate |
| PP2 | 6.7 | (0.264) | Minimum | Datum 'A' to minimum Flat area on Customer Faceplate |
| QQ2 | 5.90 | (0.232) | MAX | Datum 'A' to top of Connector |
| RR2 | 13.23 | (0.521) | REF | Datum 'A' to top of cut-out in Customers Faceplate |
| SS2 | 12.2 | (0.480) | REF | Depth of surface mount connector keep-out area. |
| TT2 | 3.50 | (0.138) | ±0.50 | Height from Datum 'A' to centerline of LED bank |
| UU2 | 23.7 | (0.930) | ±0.50 | Distance from Datum 'J' to centerline of LED bank |
| RA2 | 2.00 | (0.079) | N/A | Maximum Radius of opening in Customers sheet metal Faceplate |
| RB2 | 4.00 | (0.079) | N/A | Maximum Radius on Cut-out on Customers PCB |

18.1 Transceiver Printed Circuit Board

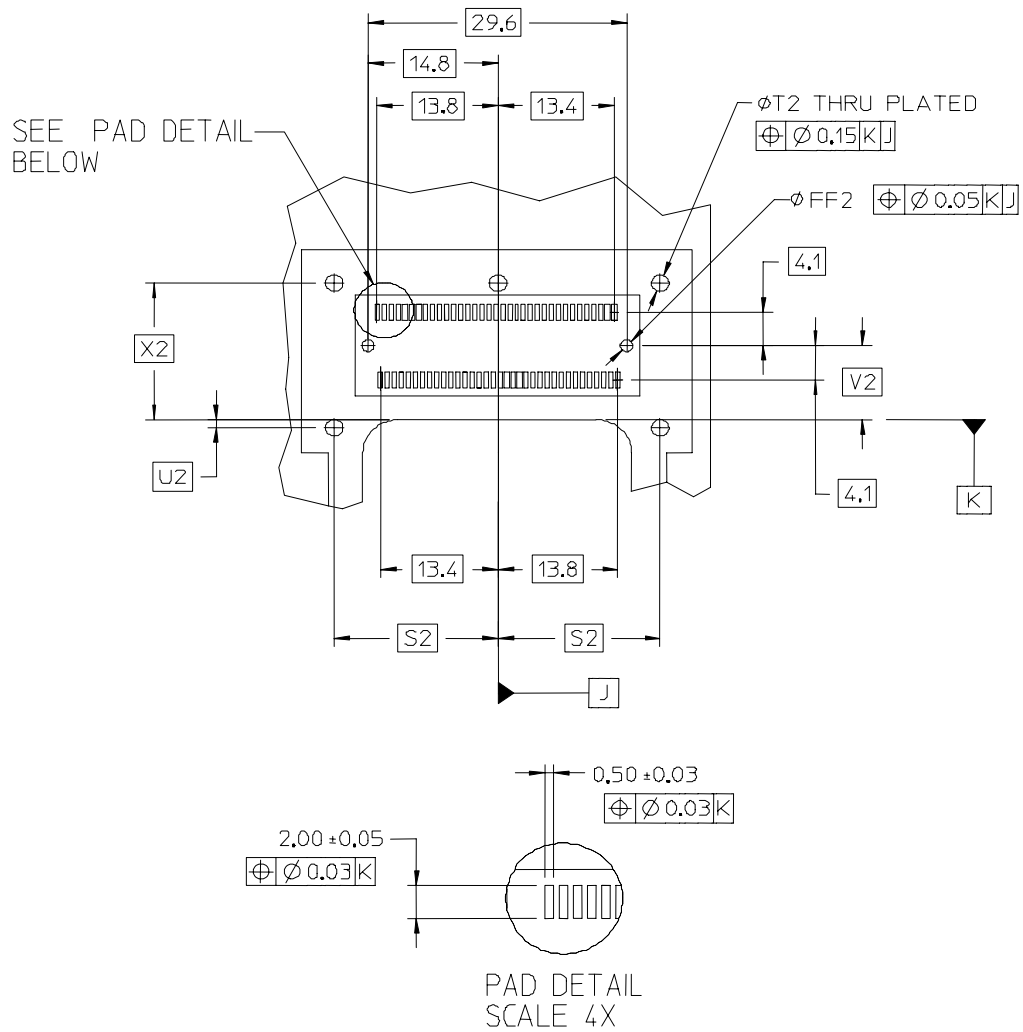
A typical contact pad plating for the printed circuit board is 0.38 micrometers minimum hard gold over 1.27 micrometers minimum thick nickel. Other plating options that meet the performance requirements are acceptable.

Fig 6. Transceiver Printed Circuit Board Connector



18.2 Host Board Mechanical Layout

Fig 7. Host Board Connector Layout



18.3 Electrical Connector

Fig 8. Connector Drawing

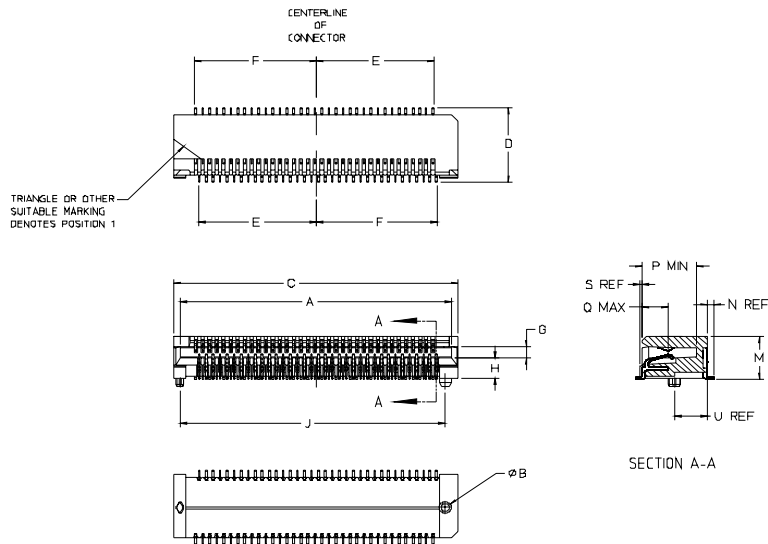


Table 3 Connector Dimensions

| Key | Dim. (mm) | Tolerance | COMMENTS |
|-----|-----------|------------|--|
| A | 29.4 | ± 0.08 | Connector card slot |
| B | 1.4 | ± 0.05 | Guide pin diameter |
| C | 31.2 | Maximum | Connector width |
| D | 9.2 | Maximum | Connector Length |
| E | 13.5 | Reference | Distance from centerline of connector to outer contact |
| F | 13.9 | Reference | Distance from centerline of connector to outer contact |
| G | 1.35 | Maximum | Connector card slot height |
| H | 2.6 | Minimum | Height from bottom of connector to bottom of card slot |
| J | 29.6 | TP | Distance between guide pins |
| K | 0.9 | Reference | Diamond guide pin width, NOT SHOWN |
| L | 1.4 | ± 0.05 | Diamond guide pin length, NOT SHOWN |
| M | 5.9 | Maximum | Connector height |
| N | 0.8 | Reference | Length of solder leads past housing, front and rear |
| P | 6.0 | Minimum | Depth of card slot from front face of housing |
| Q | 3.0 | Maximum | Depth of contact point from front face of connector |
| R | 0.7 | ± 0.01 | Size of chamfer on top of connector, NOT SHOWN |
| S | 0.3 | Reference | Distance boss extends past front face of connector |
| T | 0.6 | Minimum | Size of chamfer at entry of card slot, all around, NOT SHOWN |
| U | 4.5 | Reference | Length from centerline of guide posts to end of solder lead |

18.4 Optical Interface

The objective of this section is to specify the optical connector interface to sufficiently insure performance, intermateability and maximum supplier flexibility.

18.4.1 Optical Plug:

The optical interface shall use a duplex SC optical plug which conforms to IEC 61754-4. Only the floating duplex style connector plug shall be used. Rigid SC duplex connectors shall not be used. Connector keys are used for transmit / receive polarity.

NOTE: Floating Duplex SC Connectors use two simplex connectors and mechanically couple them together to create 1 connector that retains both, but allows both connectors to 'float', within the specified tolerance.

18.4.2 Optical Receptacle:

The SC Duplex Receptacle shall conform to the requirements of IEC 61754-4 with the following clarification:

The distance between the center line of the active optical bores (ref DB) shall be 12.25/13.15mm to match the floating duplex SC optical plug (ref Duplex optical plug table Note 8).

Increasing this tolerance avoids the restrictive manufacturing tolerance associated with rigid SC connectors.

19 Thermal Requirements

The purpose of this section is to define the limiting or boundary conditions to help efficient thermal system design.

Substantial variations in module thermal performance can occur depending on system level thermal design.

The parameters defined in this section shall enable clear communication of any thermal simulation or thermal test data between module supplier and system vendor and will aid correlation between simulation and actual measured results

This document however does not guarantee system level performance or port density that will be resolved on a system specific basis.

Any characterization results presented in this thermal section are given as examples only.

19.1 Maximum power dissipation

The 850nm or 1310nm PMDs will dissipate a maximum 6W.
The 1550nm PMD will dissipate a maximum 10W.

19.2 System design & assumptions for characterisation, simulations and measurements

Information presented by the module vendor in relation to this document will be obtained from a 'confined or ducted flow' system as shown in figures 9 and 10.

A blower duct is mounted so that the direction of airflow is parallel to the heat sink fins. Pressure and airflow measurement points are shown.

Airflow should be characterized using a calibrated hot wire anemometer placed at the airflow inlet (A7) and system pressure drop should be measured at points P1 and P2 with calibrated micro-manometers.

Thermocouples should be used to measure case temperatures.

Each module vendor as a minimum requirement will be provide measurement data, defined as mandatory, in Table 5.

Identical PMD types will be expected to be characterized I.E. no mix of 850nm or 1310nm or 1550nm PMDs is mandated.

A minimum of 8 of 850nm or 1310nm PMDs will be tested whereas a minimum of 4, 1550nm parts are to be tested.

When undergoing thermal evaluation XENPAK transceivers should output idle patterns on both the XAUI and PMD outputs. The idle patterns for XAUI and PMD are described in IEEE802.3ae sections 48.2.4.2 and 49.2.4.7 respectively.

Other measurement data provided is at the discretion of the vendor.

19.2.1 Test Environment

- Uniform airflow will exist across the vent opening and will be of constant volume airflow.
- Altitude (sea level)
- Air humidity (50% \pm 10)
- Inlet Air temperature (25C \pm 1)

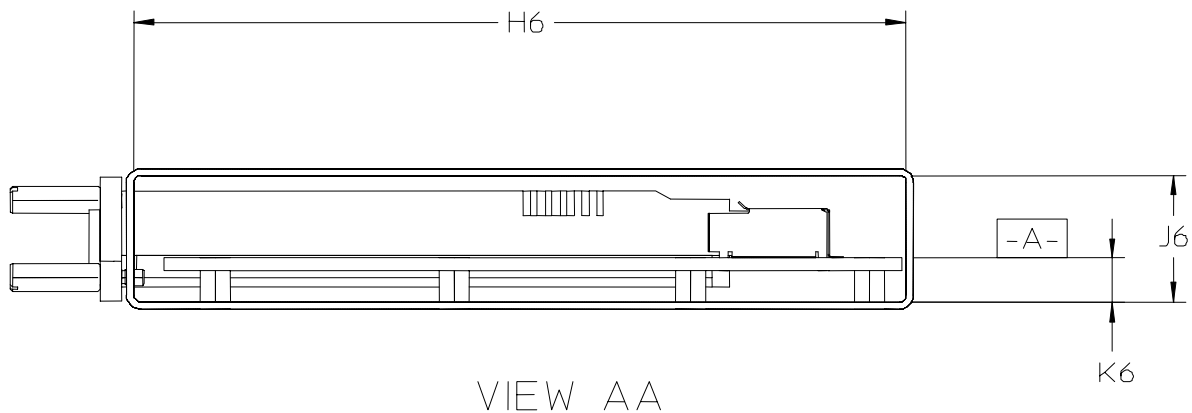
19.2.2 Test fixture

- PCB motherboard must be 2mm thick \pm 0.2mm and have no copper content between datum B and datum F except for a 4mm chassis ground, as shown in Fig 5.
- Space for an EMI shield as included in the MSA should be provided.
- A wind tunnel housing with poor thermal conduction will be used - a plastic (IR transparent to allow the potential use of an infrared camera) is recommended.
- Dimensions of system and other features are represented in the drawings documenting the test unit
- For the multiple module configuration it is assumed that the conditions drawn for module 1 will be duplicated for module n. i.e. the EMI shield will be present for all modules.
- Blanking plates will be provided to close the front faceplate when modules are not inserted in test chamber slots but they will not fill the slot in the test pcb.
- For multiple module tests the modules will all be adjacent to one another with no gaps from empty test chamber slots.
- The test chamber will be clear of obstruction for 30cm after the outlet.

Module conditions

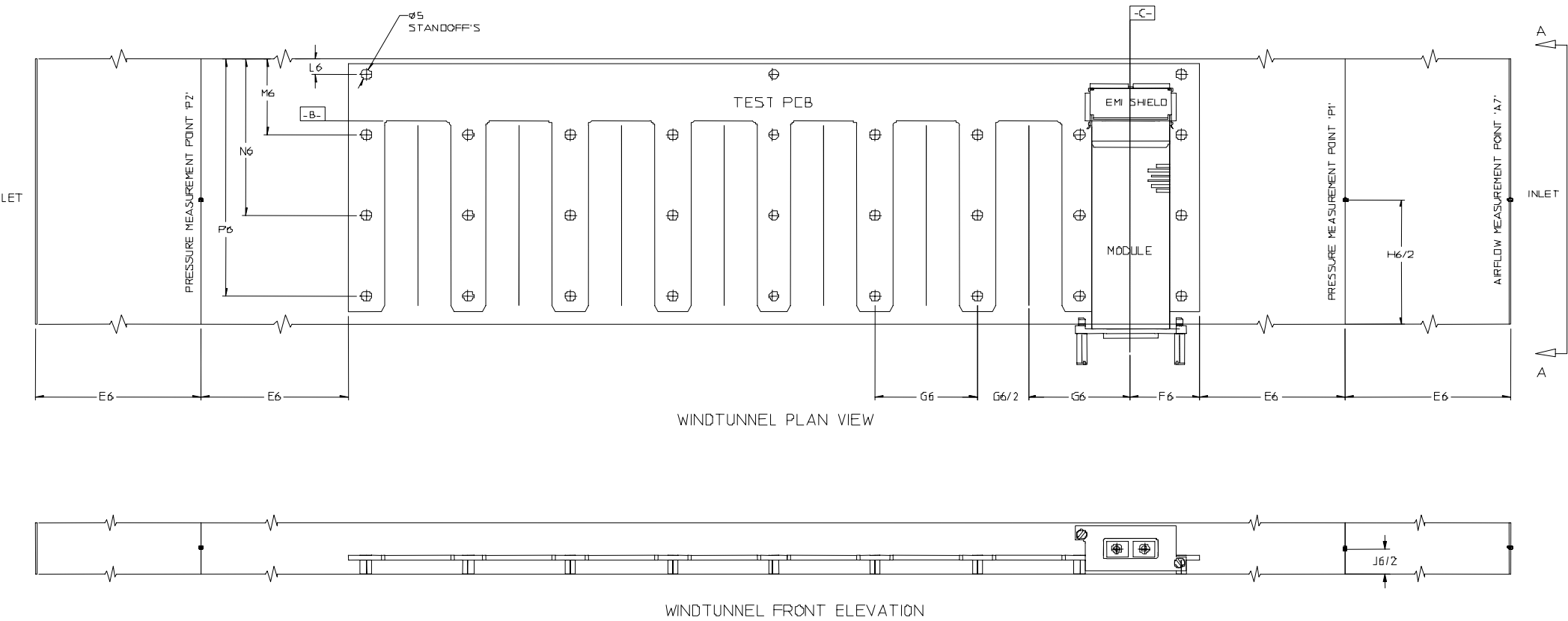
-
- A steady state should be obtained to take measurements.

**Fig 9. Cross Section of Test Fixture
SEE Table 4 FOR DIMENSIONS**



System design & assumptions for characterization, simulations and measurements (cont'd).

Fig 10. Plan and Side view of Test Fixture
SEE Table 4 FOR DIMENSIONS

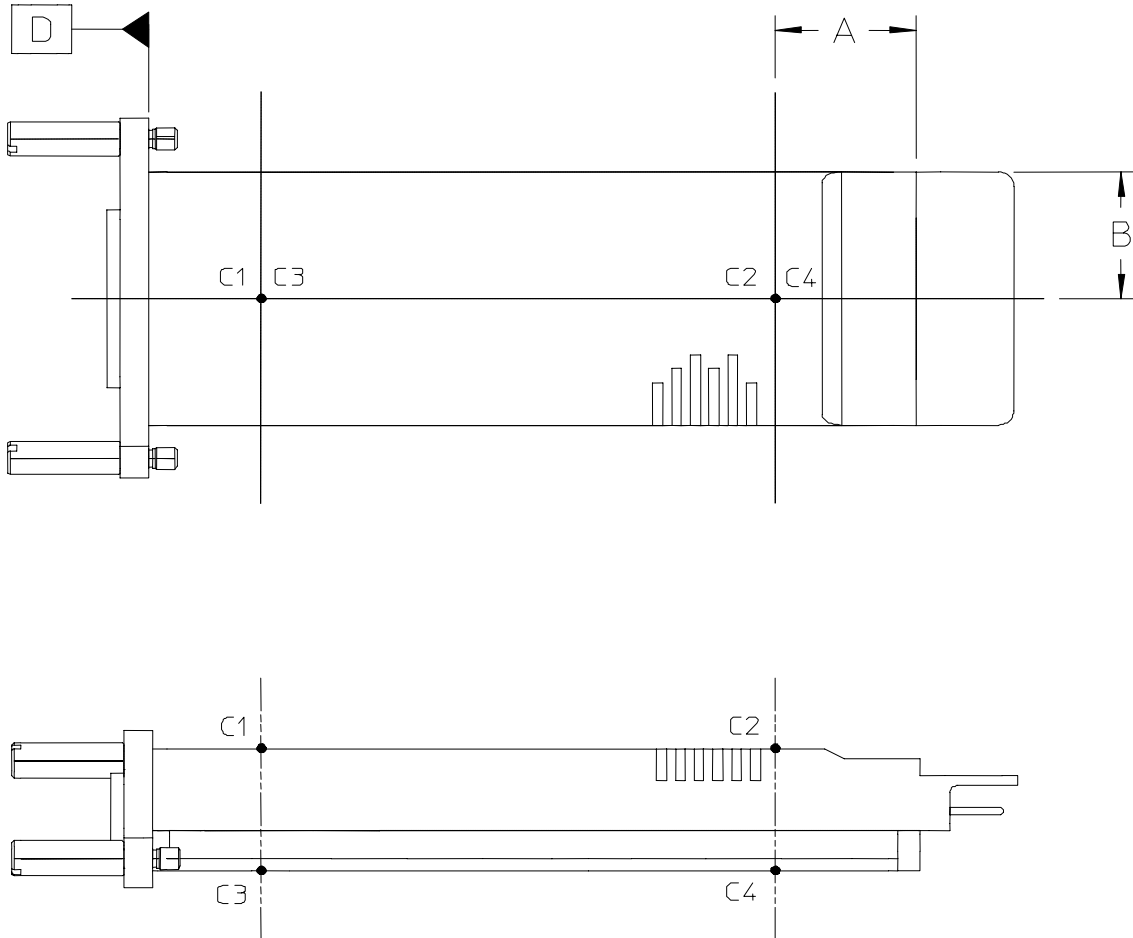


19.2.3 Measurement Positions

Positions where case temperatures will be measured are described below. These will be the reference points for thermal results that will be referred to in supplier data sheets.

As a minimum each supplier shall provide test data for the mandatory test points for temperature defined in Table 5.

**Fig 11. Mandatory temperature measurement points
SEE Table 5 FOR DIMENSIONS**



19.2.4 Optional Airflow measurement points

To aid correlation of vendor simulation to vendor system test data, optional test points for airflow measurement have been defined, in close proximity to the module, as listed in Table 4 and are shown in Fig 12 below.

**Fig 12. Optional air flow measurement points
SEE FOR Table 6 DIMENSIONS**

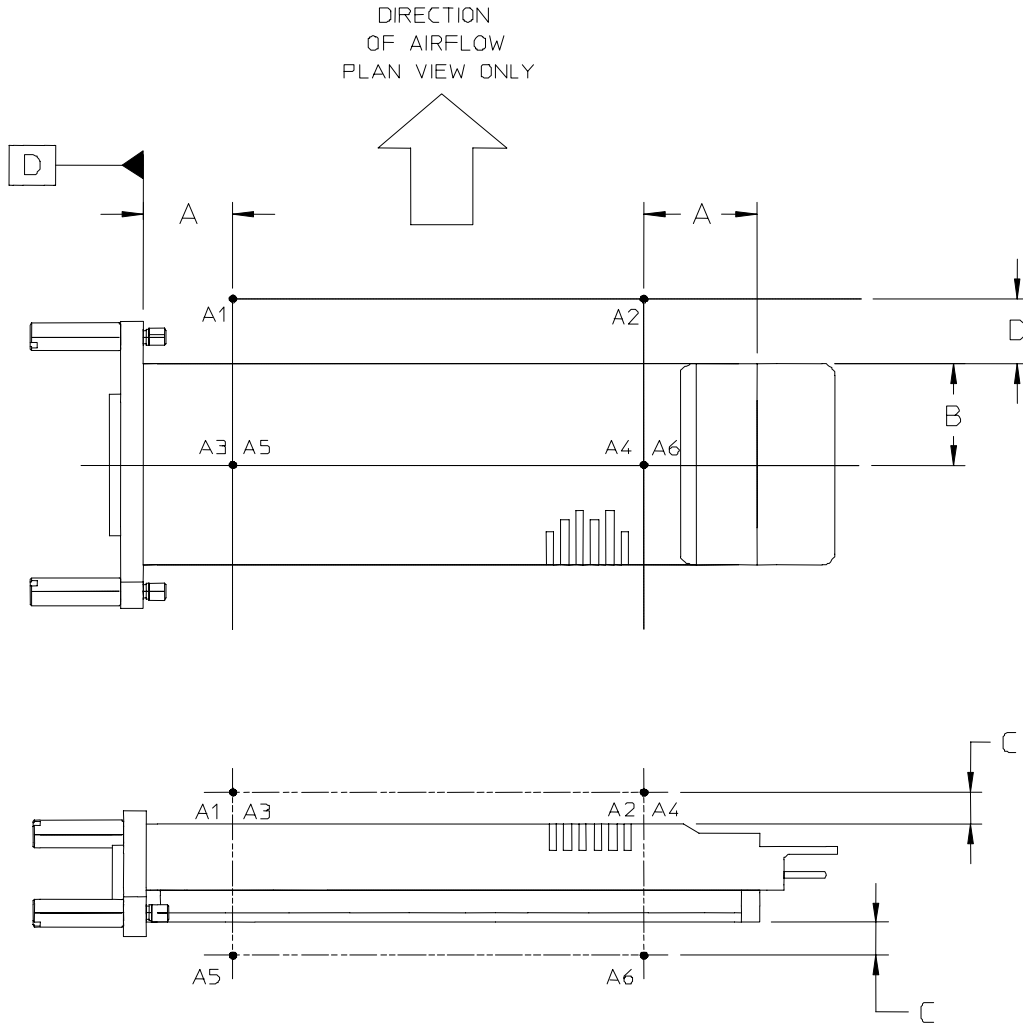


Table 4 Test chamber conditions and test-points locations

| Key | Dim. (mm) | Tolerance | COMMENTS |
|-----|-----------|-----------|--|
| A | 25.0 | ± 2.0 | |
| B | 18 | ± 2.0 | |
| C | 2.0 | ± 0.5 | |
| D | 4.24 | ± 2.0 | |
| E6 | 152.4 | ± 1.0 | Spacing for measurement points |
| F6 | 32.0 | ± 1.0 | Datum [-C-] to edge of customers PCB |
| G6 | 47.47 | BASIC | Minimum Module spacing |
| H6 | 130.0 | ± 1.0 | Width of inside Windtunnel |
| J6 | 23.0 | ± 1.0 | Height of Windtunnel |
| K6 | 7.95 | ± 1.0 | Datum [-A-] to bottom inside surface of Windtunnel |
| L6 | 7.50 | ± 1.0 | Mounting spacer |
| M6 | 37.50 | ± 1.0 | Mounting spacer |
| N6 | 77.50 | ± 1.0 | Mounting spacer |
| P6 | 117.50 | ± 1.0 | Mounting spacer |

Table 5 Mandatory Results

| | | | |
|-----------------------|-----------------------|---------------|--|
| A7 | | +/-2.0 | <i>Mandatory Airflow test point</i> |
| C1, C2, C3, C4 | - | - | <i>Mandatory Case temperature test points</i> |
| P1 | E6, H6/2, J6/2 | ± 2.0 | <i>Mandatory Air pressure test point</i> |
| P2 | E6, H6/2, J6/2 | ± 2.0 | <i>Mandatory Air pressure test point</i> |

Table 6 Optional Results for correlation.

| | | | |
|----------------------|---|---|---|
| A1, A2 | - | - | Optional Air flow simulation or measurement test points |
| A3,A4, A5, A6 | - | - | Optional Air flow simulation test points |

19.2.5 Example test data

Mandatory data collected according to Table 5 will be represented in charts as described in the example charts below.

Fig 13. Case temperature vs. Airflow (A7).

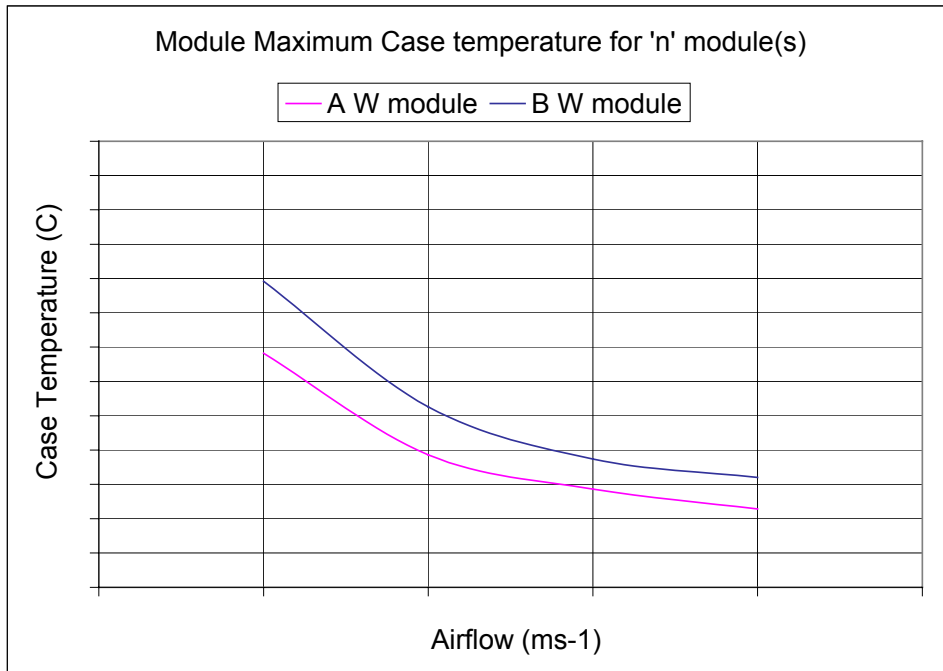
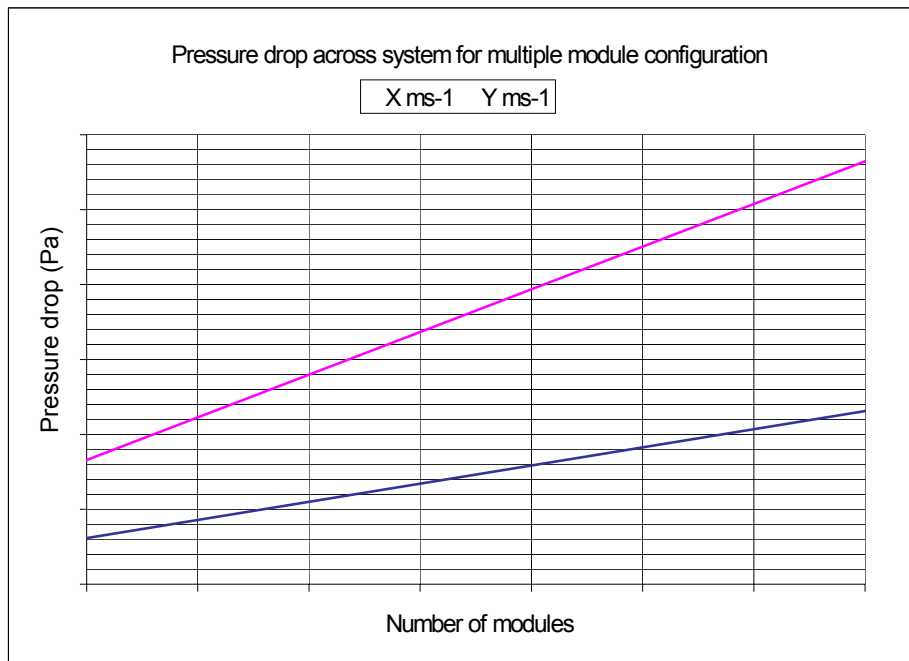


Fig 14. Pressure drop vs. number of modules with respect to airflow



20 XENPAK Electrical Interface

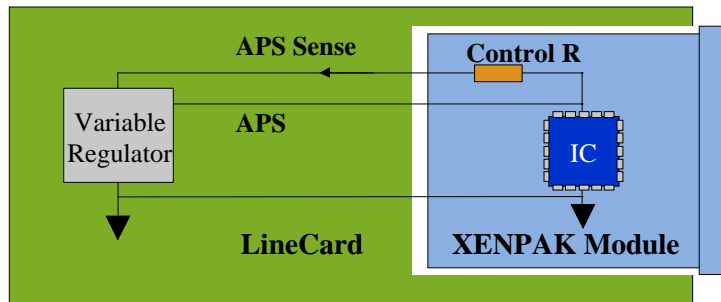
20.1 Power Supplies and Hot Swapping

5.0V, 3.3V and an adaptable power supply rail (APS) are available on the transceiver connector. During module insertion chassis ground contacts first to the customer chassis via the chassis areas defined in **Fig 5** on the host board. The first electrical connector pins to make contact are Electrical Ground followed by VCC and Signal contacts that mate simultaneously. There is no advantage in mating VCC before signal since the Hot Swap ramp time is considerably longer than any likely mechanical insertion time. For this reason the 10G transceiver should tolerate biasing of signal contacts in the absence of VCC.

20.2 Grounding

Chassis and electrical ground will be DC-isolated.

20.3 Adaptable Power Supply Adaptable Power Supply



The Backplane will provide an adaptable power supply capable of adjusting from a high of 1.8 volts to a low of 0.9 volts to the connector pins defined as the “adaptable voltage in Table 7

The XENPAK module shall support a Kelvin connection (voltage sense pin) on connector pin labeled APS Sense Connection in Table for the adaptable supply.

The XENPAK module shall incorporate a resistor between the APS Sense Connection and the adaptable voltage power plane within the XENPAK module. Resistor values, corresponding to the required voltage, shall be as in Table 7. It is recommended that this resistor be connected from the APS Sense Connection to a point on the XENPAK module near the device(s) being powered. This allows the Adaptable supply to compensate for undesired voltage drops across the backplane itself and the XENPAK connector.

The backplane will provide approximately 0V to the adaptable voltage rail when no XENPAK module (i.e. infinite impedance) is installed and will ramp up to the requested voltage when the XENPAK module with the programming resistor is installed.

Table 7 Adaptable Power supply reference

| Module Target Voltage | Control R |
|-----------------------|--------------|
| +/-3.0% | +/-0.1% |
| <i>Volts</i> | <i>Kohms</i> |
| 1.8 | 0.0 |
| 1.5 | 0.392 |
| 1.3 | 0.649 |
| 1.2 | 0.787 |
| 1.1 | 0.909 |
| 1.0 | 1.05 |
| 0.9 | 1.18 |
| 0.0 | None |

20.3.1 Adaptable Power Supply Specs/Requirements

The backplane will provide a steady state voltage on the adaptable voltage power plane within an error of $\pm 3\%$ of the target value.

The steady state RMS ripple from the backplane supply will be $<40\text{mV rms}$.

The voltage overshoot on the adaptable voltage power plane during the hot plug operation overshoot will be $< 3\%$ of the steady state target.

The XENPAK module shall be fully functional within 5 seconds after the adaptable power supply backplane has stabilized to within the aforementioned $\pm 3\%$ levels. If the module contains optical components requiring longer than the 5 second period to stabilize, then this requirement shall be interpreted to be exclusive of those specific optical parameter(s), for example laser line width. (Because this event is initiated by a human action of plugging in the module, another 5 seconds more or less should not matter. 5 seconds gives time to slow ramp currents with simple circuits and plenty of oscillator warm up and reset time).

The inrush current on the adaptable voltage rail will be limited by the adaptable backplane and supply therefore no specific inrush control is required for the adaptable voltage rail on the XENPAK module. To allow this, the XENPAK module shall be constrained to applying less than 200 μf total capacitance between the adaptable voltage rail and ground.

A XENPAK module inserted in this system shall add $<20\text{mV rms}$ ripple onto the adaptable voltage connector pins at all times. The test circuit for this measurement shall be an ideal, or near ideal voltage source followed by a 5 ohm series resistor.

20.4 Fixed Voltage Supply Specs and Inrush Currents

These specifications shall be applicable to the fixed 3.3V and 5.0V supply rails.

The inrush current on any fixed supply rail during hot plug of a XENPAK module shall be limited by the XENPAK module to assure a maximum current draw of less than 0.5 amps per power connector pin.

The inrush current on any fixed supply rail during hot plug of a XENPAK module shall be limited by the XENPAK module to assure a maximum rate of change of less than 50 milliamperes per millisecond.

Discussion: This requirement is intended to prevent the hot plug operation from disturbing the operation of previously installed XENPAK modules in the same rack. Even if the inrush is capped we must allow time for the supply to adjust for the increased load so that operating modules do not see a supply voltage drop due to a rapid current change. If the inrush rate of change is very fast, the supply will not adjust fast enough, the energy for the new module will come from the adjacent module and the adjacent module can crash regardless of current overshoot. Details depend on many variables and the estimated 50 milliamperes per millisecond may need to be adjusted contingent upon further development of the backplane and power modules.

Ramp up time controlled by the XENPAK module shall be consistent with allowing operation with 5 seconds after the adaptable power supply backplane has stabilized as required above.

The backplane will provide a steady state voltage on the fixed voltage power plane within an error of $\pm 3\%$ of the target value.

The steady state rms ripple from the backplane supply will be $<40\text{mV rms}$.

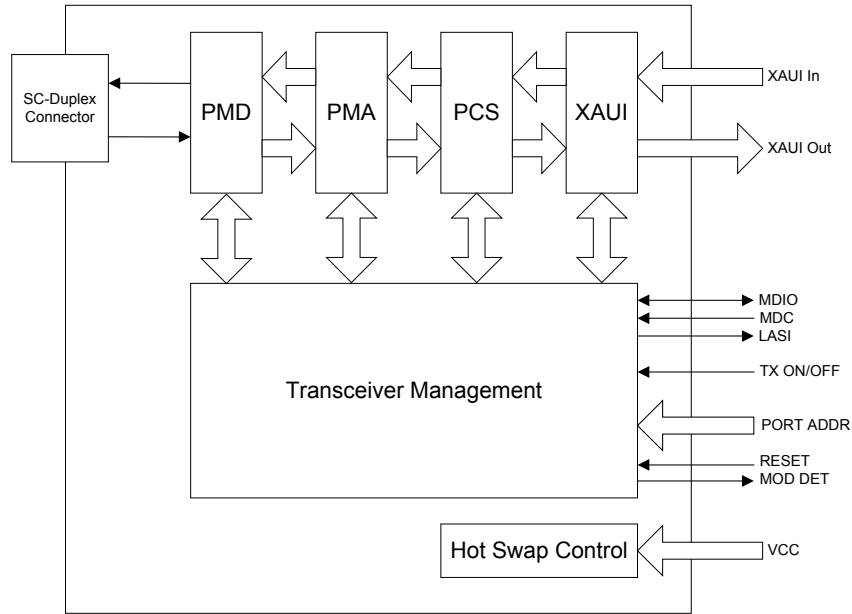
A XENPAK module inserted in this system shall add $<20\text{mV rms}$ ripple onto the fixed voltage connector pins at all times. The test circuit for this measurement shall be an ideal, or near ideal voltage source followed by a 5 ohm series resistor.

20.5 Transceiver Monitoring

Contacts are available on the module connector for Link Alarm Status Interrupt (LASI). A module detect pin allows hardware detection of a module when it is inserted into a customer chassis. This pin is pulled through 1kΩ to GND inside the module and can be used to drive an interrupt for polling-free module detection.

The 2-wire Management Data I/O interface (802.3ae Clause 45) is mandatory in the XENPAK MSA. MDC provides clocking for the data which is passed on the MDIO line. Five further pins allow for loading of a Port Address (PRTAD0-4) into the module.

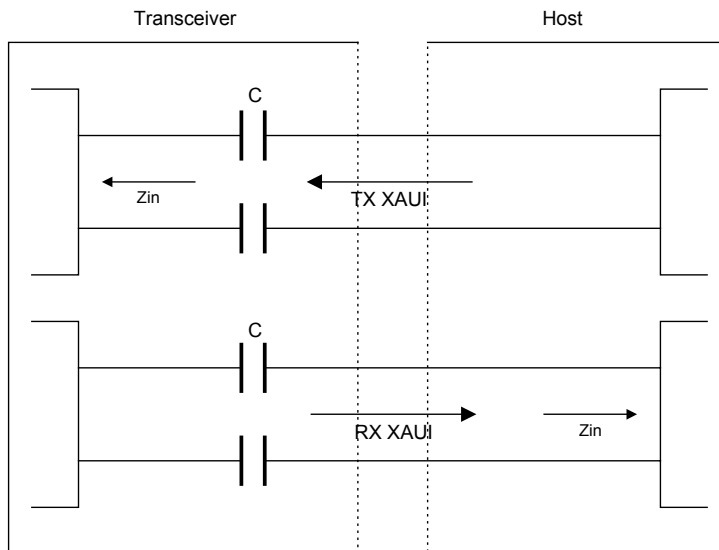
Fig 15. Functional Diagram of Typical XENPAK Style Transceiver



20.5.1 High Speed Signals

The XAUI transmit and receive data complies with IEEE802.3ae Clause 47 electrical specification, which should be referenced for actual values. AC coupling is provided inside the module for both transmit and receive directions as indicated in Fig 16. For clarity only one TX and RX XAUI lane is shown.

Fig 16. High Speed Signals



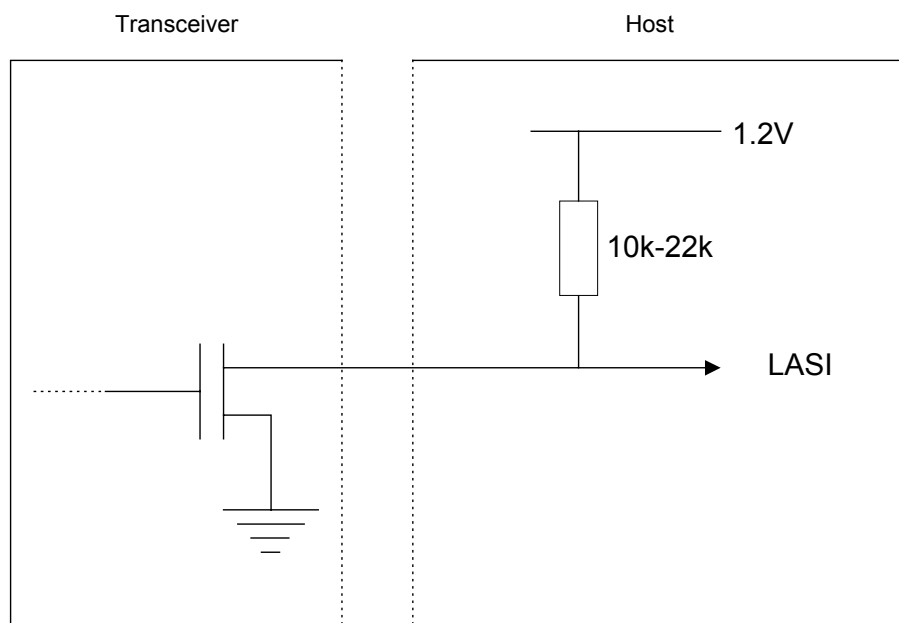
20.5.2 Low Speed Signals

Low Speed Signals are open drain compatible. Pull up resistors are provided in the transceiver or on the host board according to Table 8.

Table 8 Electrical Characteristics of Low Speed Interface

| Parameter | Min | Typ | Max | Units | Notes |
|--------------------|------|-----|------|----------|--|
| $V_{IL(MAX)}$ | - | - | 0.36 | V | 1.2V CMOS |
| $V_{IH(MIN)}$ | 0.84 | - | 1.25 | V | 1.2V CMOS |
| Capacitance | - | - | 320 | pF | Maximum Fanout of 32. 10pF per port |
| Pull Up Resistance | 10k | | 22k | Ω | |

Fig 17. Example of Low Speed Output Configuration



20.5.3 Hot Swap and Transceiver Power-On-Reset Definition

When a 10G transceiver is inserted the peak inrush currents to any supply rail shall not exceed the steady state currents for that rail by more than 50%. The ramp rate of supply current must also comply with the specification in Table 1. Inrush current control should be internal to the XENPAK transceiver.

The 10G transceiver shall achieve a stable state of normal operation after mechanical insertion at time, $t=0$ according to the following specification. After successful initialization the transceiver should clear Bit 15 in MDIO register 1.0. A timing diagram is in Fig 18.

Table 9 Power on Reset characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---------------------|-----------------|------|------|------|-------|
| Icc Peak Inrush | $I_{CC_{PEAK}}$ | - | - | 50 | % |
| Icc Ramp rate | dI_{CC}/dt | - | - | 50 | mA/ms |
| Initialisation Time | t_{init} | - | - | 5 | s |

Fig 18. Initialisation and Hot Swap Timing Diagram

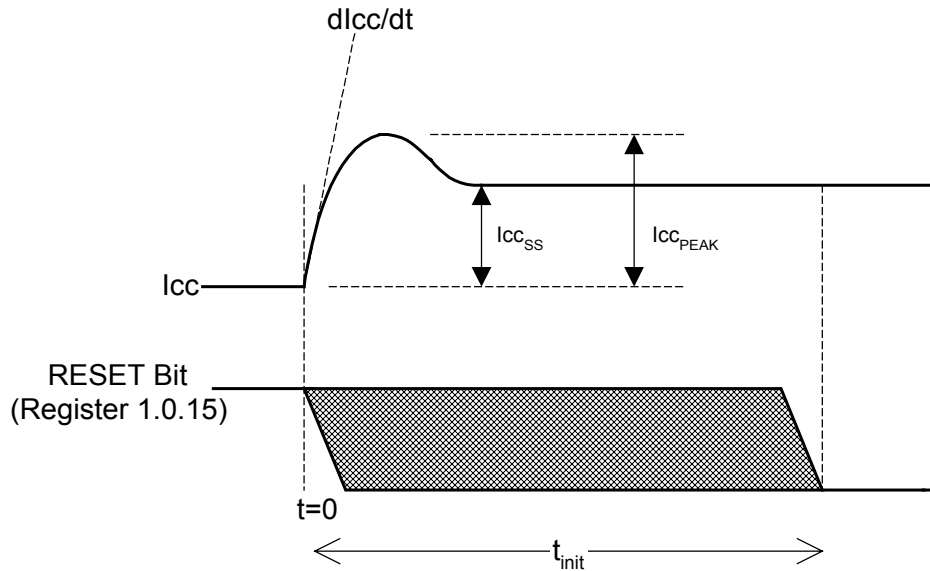


Table 10 Relationship between the TRANSCEIVER RESET pin and MDIO Reset Bit

| RESET Pin | MDIO Register Condition 1.0.15 | Transceiver Behaviour |
|-----------|--------------------------------|-----------------------|
| 1 | 0 | Normal operation |
| 0 | 0 | Reset |
| 1 | 1 | |
| 0 | 1 | |

20.6 Multiple PMD Support

This MSA aims to accommodate all four 10Gb PMDs and future WAN implementations. Clock inputs and outputs are provided with the latter in mind. It is not expected that external clocking should be used by transceivers operating in the LAN domain. Clock input and output pins are for further study.

For 10GBASE-LX4 the wavelength to lane mapping is as follows:

Table 11 LX4 Lane Mapping

| Lane | Wavelength Range/nm |
|------|---------------------|
| 0 | 1269.0 - 1282.4 |
| 1 | 1294.5 -1307.9 |
| 2 | 1320.0 - 1333.4 |
| 3 | 1345.5 - 1358.9 |

Wavelengths will always be mapped to the XAUI interface so that the longer the wavelength the higher the XAUI lane number.

20.7 Connector

The XENAPAK connector is a 70-way two-row connector (TycoAMP Part No. 1367337-1 or equivalent) which is similar in style to the 20-way SFP connector.

The 10G transceiver PCB forms one mating half of the connector.

Pin definitions are listed in Table 12 and Table 13.

Mechanical dimensions for the transceiver Electrical Pad Layout and Host board are shown in Section 18,. Layouts are shown in Fig 19 and Fig 20

20.8 ESD

Human Body Model survivability is recommended to a minimum of 500V, measured to MIL STD 883 Method 3015.1. End of row contacts on the transceiver connector are ground connections so that I/O pins will not be subjected to the highest Charged Device Model (CDM) ESD test voltage, if applicable.

Table 12 Pin Function Definitions (Lower Row)

| Pin No | Name | Dir | Function | Notes |
|--------|---------------|-----|---|-------|
| 1 | GND | | Electrical Ground | 1 |
| 2 | GND | | Electrical Ground | 1 |
| 3 | GND | | Electrical Ground | 1 |
| 4 | 5.0V | | Power | 2 |
| 5 | 3.3V | | Power | 2 |
| 6 | 3.3V | | Power | 2 |
| 7 | APS | | Adaptive Power Supply | 2 |
| 8 | APS | | Adaptive Power Supply | 2 |
| 9 | LASI | | Open Drain Compatible 10K-22K pull up on host. Logic High: Normal Operation Logic Low: LASI Asserted | 4 |
| 10 | RESET | I | Logic High: Normal Operation, Low: Reset | 4 |
| 11 | VEND SPECIFIC | | Vendor Specific Pin. Leave unconnected when not in use. | 8 |
| 12 | TX ON/OFF | I | Open Drain compatible. 10-22K pull-up on transceiver Logic high = Transmitter On Logic low = Transmitter Off | 4 |
| 13 | RESERVED | O | Reserved | 4 |
| 14 | MOD DETECT | O | Pulled low inside module through 1k | |
| 15 | VEND SPECIFIC | | Vendor Specific Pin. Leave unconnected when not in use. | 8 |
| 16 | VEND SPECIFIC | | Vendor Specific Pin. Leave unconnected when not in use. | 8 |
| 17 | MDIO | I/O | Management Data IO | 4 |
| 18 | MDC | I | Management Data Clock | 4 |
| 19 | PRTAD4 | I | Port Address Bit 4 | 4 |
| 20 | PRTAD3 | I | Port Address Bit 3 | 4 |
| 21 | PRTAD2 | I | Port Address Bit 20 | 4 |
| 22 | PRTAD1 | I | Port Address Bit 10 | 4 |
| 23 | PRTAD0 | I | Port Address Bit 0 | 4 |
| 24 | VEND SPECIFIC | | Vendor Specific Pin. Leave unconnected when not in use. | 8 |
| 25 | RESERVED | | Reserved | |
| 26 | RESERVED | | Reserved for Avalanche Photodiode use. | 8 |
| 27 | APS SENSE | | APS Sense Connection | |
| 28 | APS | | Adaptive Power Supply | 2 |
| 29 | APS | | Adaptive Power Supply | 2 |
| 30 | 3.3V | | Power | 2 |
| 31 | 3.3V | | Power | 2 |
| 32 | 5.0V | | Power | 2 |
| 33 | GND | | Electrical Ground | 1 |
| 34 | GND | | Electrical Ground | 1 |
| 35 | GND | | Electrical Ground | 1 |

Table 13 Pin Function Definitions (Upper Row)

| Pin No | Name | Dir | Function | Notes |
|--------|-----------|-----|----------------------------|-------|
| 36 | GND | | Electrical Ground | 1 |
| 37 | GND | | Electrical Ground | 1 |
| 38 | RX CLK+ | O | Reserved for WAN Phy | 6 |
| 39 | RX CLK- | O | Reserved for WAN Phy | 6 |
| 40 | GND | | Electrical Ground | 1 |
| 41 | RX LANE0+ | O | Module XAUI Output Lane 0+ | 7 |
| 42 | RX LANE0- | O | Module XAUI Output Lane 0- | 7 |
| 43 | GND | | Electrical Ground | 1 |
| 44 | RX LANE1+ | O | Module XAUI Output Lane 1+ | 7 |
| 45 | RX LANE1- | O | Module XAUI Output Lane 1- | 7 |
| 46 | GND | | Electrical Ground | 1 |
| 47 | RX LANE2+ | O | Module XAUI Output Lane 2+ | 7 |
| 48 | RX LANE2- | O | Module XAUI Output Lane 2- | 7 |
| 49 | GND | | Electrical Ground | 1 |
| 50 | RX LANE3+ | O | Module XAUI Output Lane 3+ | 7 |
| 51 | RX LANE3- | O | Module XAUI Output Lane 3- | 7 |
| 52 | GND | | Electrical Ground | 1 |
| 53 | GND | | Electrical Ground | 1 |
| 54 | GND | | Electrical Ground | 1 |
| 55 | TX LANE0+ | I | Module XAUI Input Lane 0+ | 7 |
| 56 | TX LANE0- | I | Module XAUI Input Lane 0- | 7 |
| 57 | GND | | Electrical Ground | 1 |
| 58 | TX LANE1+ | I | Module XAUI Input Lane 1+ | 7 |
| 59 | TX LANE1- | I | Module XAUI Input Lane 1- | 7 |
| 60 | GND | | Electrical Ground | 1 |
| 61 | TX LANE2+ | I | Module XAUI Input Lane 2+ | 7 |
| 62 | TX LANE2- | I | Module XAUI Input Lane 2- | 7 |
| 63 | GND | | Electrical Ground | 1 |
| 64 | TX LANE3+ | I | Module XAUI Input Lane 3+ | 7 |
| 65 | TX LANE3- | I | Module XAUI Input Lane 3- | 7 |
| 66 | GND | | Electrical Ground | 1 |
| 67 | TX CLK+ | I | Reserved for WAN Phy | 6 |
| 68 | TX CLK- | I | Reserved for WAN Phy | 6 |
| 69 | GND | | Electrical Ground | 1 |
| 70 | GND | | Electrical Ground | 1 |

Notes:

- 1) Ground connections are common for TX and RX.
- 2) VCC contacts are each rated at 0.5A nominal.
- 3) Timing characteristics for further study but expected to be the same as SFP.
- 4) 1.2V CMOS compatible.
- 5) MDIO and MDC timing must comply with IEEE802.3ae, Clause 45.3
- 6) Clock Input and Output characteristics for further study.
- 7) XAUI output characteristics should comply with IEEE802.3ae Clause 47.
- 8) Transceivers will be MSA compliant when no signals are present on the vendor specific pins.
- 9) Minimum delay from TX "off" to loss of optical power 100us, TX on or off, minimum pulse width 100us

Fig 19. XENPAK Transceiver Electrical Pad Layout

| | | | |
|----|-----------|----|---------------|
| 70 | GND | 1 | GND |
| 69 | GND | 2 | GND |
| 68 | TX CLK- | 3 | GND |
| 67 | TX CLK+ | 4 | 5.0V |
| 66 | GND | 5 | 3.3V |
| 65 | TX LANE3- | 6 | 3.3V |
| 64 | TX LANE3+ | 7 | APS |
| 63 | GND | 8 | APS |
| 62 | TX LANE2- | 9 | LASI |
| 61 | TX LANE2+ | 10 | RESET |
| 60 | GND | 11 | VEND SPECIFIC |
| 59 | TX LANE1- | 12 | TX ON/OFF |
| 58 | TX LANE1+ | 13 | RESERVED |
| 57 | GND | 14 | MOD DETECT |
| 56 | TX LANE0- | 15 | VEND SPECIFIC |
| 55 | TX LANE0+ | 16 | VEND SPECIFIC |
| 54 | GND | 17 | MDIO |
| 53 | GND | 18 | MDC |
| 52 | GND | 19 | PRTAD4 |
| 51 | RX LANE3- | 20 | PRTAD3 |
| 50 | RX LANE3+ | 21 | PRTAD2 |
| 49 | GND | 22 | PRTAD1 |
| 48 | RX LANE2- | 23 | PRTAD0 |
| 47 | RX LANE2+ | 24 | VEND SPECIFIC |
| 46 | GND | 25 | RESERVED |
| 45 | RX LANE1- | 26 | RESERVED |
| 44 | RX LANE1+ | 27 | APS SENSE |
| 43 | GND | 28 | APS |
| 42 | RX LANE0- | 29 | APS |
| 41 | RX LANE0+ | 30 | 3.3V |
| 40 | GND | 31 | 3.3V |
| 39 | RX CLK- | 32 | 5.0V |
| 38 | RX CLK+ | 33 | GND |
| 37 | GND | 34 | GND |
| 36 | GND | 35 | GND |

Top of Transceiver PCB

**Bottom of Transceiver PCB
(as viewed through top)**

20.9 Management Interface

XENPAK transceivers support the MDIO interface specified in IEEE802.3ae Clause 45. In addition to the appropriate registers to support the IEEE standard there are some registers specific to XENPAK.

20.9.1 Transceiver Identification

Efficient use of XENPAK and its specific registers requires an end-user system to recognise a connected transceiver as being of the XENPAK type. The method described in section 20.9.2. utilises the Organisationally Unique Identifier as a means not only of identifying XENPAK but also of determining the location XENPAK specific registers.

20.9.2 OUI Method

Following successful hot plugging of a XENPAK transceiver into an empty port the system software interrogates the MDIO interface for the port. A XENPAK transceiver indicates its presence by placing a XENPAK specific OUI into MDIO registers 1.11 and 1.12. Upon recognizing the XENPAK OUI the system software can initialize an appropriate management routine.

More detailed information about the XENPAK transceiver is then obtained via a secondary OUI called the Vendor OUI and this is contained within XENPAK specific Non-Volatile Registers (NVR). The NVR itself is located in one Device only. It is suggested that Devices 1-5 and 31 are used as possible containers for the XENPAK NVR since only these Devices are expected to be contained within the transceiver housing.

Software redirection to the Vendor OUI is provided by a NVR pointer contained in the XENPAK OUI. The pointer resides in the 6 bit OUI field traditionally allocated to Model Number.

Figure x. shows diagrammatically how the XENPAK OUI and Vendor OUI are used. Fig 22. shows the format of the XENPAK OUI and its relation to the Form Factor Identifier registers 1.11 and 1.12.

Fig 21. Transceiver Identification after Hot Plugging

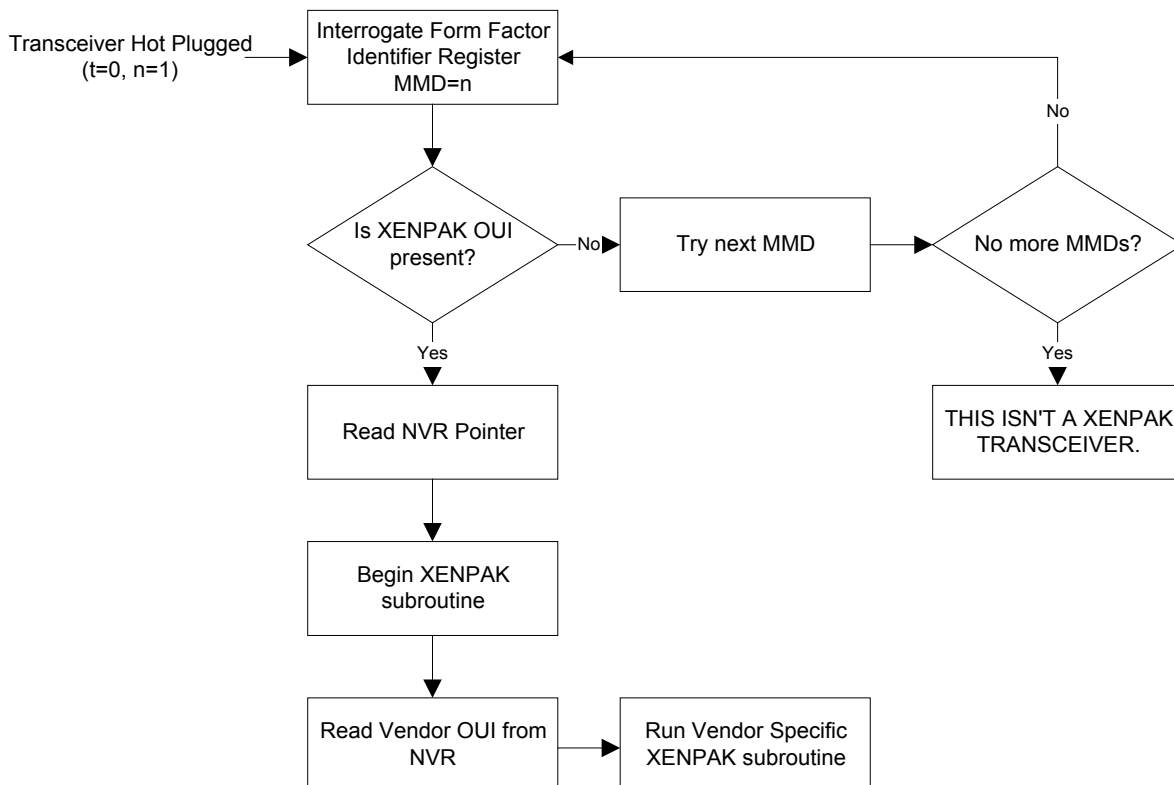


Fig 22. XENPAK OUI format

| MDIO Register 1.11 (Form Factor Identifier) | | | | | | | | | | | | | | MDIO Register 1.12 (Form Factor Identifier) | | | | | | | | | | | | | | | | | |
|---|----|----|----|----|----|---|----|----|----|----|----|----|----|---|----|----|----|----|----|----|-----------------|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 5 | 4 | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 |
| XENPAK OUI bit | | | | | | | | | | | | | | NVR Pointer | | | | | | | Rev. no. | | | | | | | | | | |

20.9.3 XENPAK Register Set

The complete XENPAK register set is shown in Table 14.

Table 14 XENPAK Register Set
Address Description

| | |
|--|--|
| 0x8000 | NVR Control/Status |
| 0x8001 to 0x8006 | Vendor Specific |
| 0x8007 to 0x8106 | Non-Volatile Registers |
| 0x8107 to 0x8806 | Vendor Specific Non-Volatile Registers |
| 0x8807 to 0x8FFF | Reserved |
| 0x9000 0x9001 0x9002 0x9003 0x9004 0x9005 | RX_ALARM Control TX_ALARM Control LASI Control RX_ALARM Status TX_ALARM Status LASI Status |
| 0x9006 to 0x9FFF | Reserved |
| 0xA000 to 0xA003 | Diagnostic Capabilities, Channels 0-3 |
| 0xA004 to 0xA00F | Reserved |
| 0xA010 to 0xA013 | Diagnostic Alarms, Channels 0-3 |
| 0xA014 to 0xA01F | Reserved |
| 0xA020 0xA021 0xA022 0xA023 0xA024 0xA025 | Laser Temperature, Channel 0 Laser Bias Current, Channel 0 Laser Output Power, Channel 0 Receive Optical Power, Channel 0 Vendor Specific, Channel 0 Vendor Specific, Channel 0 |
| 0xA026 to 0xA02F | Reserved, Channel 0 |
| 0xA030 to 0xA03F | Reserved, Channel 1 |
| 0xA040 to 0xA04F | Reserved, Channel 2 |
| 0xA050 to 0xA05F | Reserved, Channel 3 |
| 0xA060 to 0xAFFF | Reserved |
| 0xB000 to 0xB07F | LSS Registers (optional) |
| 0xB800 to 0xB80F | 10GFC PMD Register (optional) |

20.9.4 Non-Volatile Registers (NVR)

20.9.5 Overview

The XENPAK module shall maintain a set of non-volatile registers (NVRs) accessible via the MDC/MDIO management port. The NVRs shall have the location and format described in 20.9.12.

The NVRs contain information regarding the transceiver capabilities, manufacturer, and version. The implementation of the NVRs is beyond the scope of the MSA.

20.9.6 Access

The NVRs may be accessed via standard MDC/MDIO transactions to address locations specified in 20.9.12. The XENPAK module shall also maintain a control/status register at offset 0x8000 with contents described in Table 15. The intent of this register is to provide facilities to read and write the NVRs in the case where indirect access is required.

Table 15 NVR Control/Status Register (0x8000)

| Bit | Description | Properties ¹ |
|------|---|-------------------------|
| 15:8 | Vendor Specific | RW |
| 7:6 | Reserved | RO |
| 5 | Read/Write Command 0 = read NVR 1 = write NVR | RW |
| 4 | Reserved (0) | RO |
| 3:2 | Command Status 00 = idle or command in progress 01 = command completed 10 = reserved 11 = command failed | RO/LH |
| 1:0 | Extended Commands 00 = Vendor Specific 01 = Vendor Specific 10 = Vendor Specific 11 = read/write all NVR contents | RW |

¹ RW = read/write, RO = read only, LH = latch high, clear on read (note that if the condition exists following register read, the bit will not be cleared).

20.9.7 Read/Write Command (bit 5)

Any write transaction to the NVR control/status register shall initiate an NVR transaction. A zero written to bit 5 initiates an NVR read. A one written to bit 5 initiates an NVR write. The extended command bits (1 and 0) determine the exact nature of the read/write operation.

Inclusion of this function permits implementations that maintain non-volatile storage in an independent location. The read function pulls the NVR contents out of non-volatile storage and maps them to the register locations specified in 20.9.12. The write function commits the contents of the NVRs to the external non-volatile storage.

20.9.8 Command Status (bits 3, 2)

Following a write to register 0x8000 (initiation of read/write command), bits 3 and 2 provide information on the status of the command. A value of 00 indicates that either a command is in progress or no new command has

been issued, 01 indicates that the command completed successfully, and 11 indicated that the command failed.

The command status is cleared when read.

20.9.9 Extended Commands (bits 1, 0)

Bits 1 and 0 supplement the basic read/write command (bit 5). A value of 11 reads and writes all NVR contents (subject to write protection, refer to 20.9.11). All other values implement vendor specific commands.

20.9.10 Error Detection

To protect against degradation in the non-volatile storage and potential errors in transfer, XENPAK data shall be protected by an 8-bit checksum as shown in 20.9.12. The checksum may be verified by the user of the XENPAK module prior to using the NVR contents.

The checksum shall be implemented as a standard complement of the sum of complements (carry-outs discarded) algorithm covering the XENPAK basic region. The vendor specific and customer scratch areas are not covered by this checksum. Error detection capability for the vendor specific and customer writable areas is beyond the scope of the MSA.

It is not mandatory for the module to verify the checksum or report that the checksum is correct or incorrect. However, if the module operation is somehow defined by the NVR contents, it is strongly recommended that automatic verification is performed prior to using the stored information.

20.9.11 Write Protection

The XENPAK basic region and vendor-specific regions are written at the time of module manufacture and shall not be altered by read/write commands. The customer writable section shall be read/write enabled.

20.9.12 NVR Register Map

The NVR register map is shown in Table 16

Table 16 NVR Register Map

| Fields | NVR Address (dec) | MDIO Address (hex) | Size | Name | Description | Value | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Hex | |
|-------------------|-------------------|--------------------|------|----------------------------|--|-------------|---|---|---|---|---|---|---|----|-----|---|
| Header | 0 | 8007 | 1 | Version | NVR Version number | | x | x | x | x | x | x | x | x | xx | |
| | 1 | 8008 | 2 | NVR_Size | NVR Size in bytes | | x | x | x | x | x | x | x | x | xx | |
| | 3 | 800A | 2 | Mem_Used | Number of bytes used | | x | x | x | x | x | x | x | x | x | |
| | 5 | 800C | 1 | Basic Addr | Basic Field Address | | x | x | x | x | x | x | x | x | x | |
| | 6 | 800D | 1 | Cust Addr | Customer Field Address | | x | x | x | x | x | x | x | x | x | |
| | 7 | 800E | 1 | Vend Addr | Vendor Field Address | | x | x | x | x | x | x | x | x | x | |
| | 8 | 800F | 2 | Ext Vend Addr | Extended Vendor Field Address | | x | x | x | x | x | x | x | x | x | |
| Basic | 11 | 8012 | 1 | Tcvr Type | Transceiver type | Unspecified | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | XENPAK | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| | | | | | | Reserved | x | x | x | x | x | x | x | x | xx | |
| | 12 | 8013 | 1 | Connector | Optical connector type | Unspecified | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | SC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| | | | | | | LC | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 | |
| | | | | | | MT-RJ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3 | |
| | | | | | | MU | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4 | |
| | | | | | | FC/PC | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 5 | |
| | | | | | | Pigtail | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 6 | |
| | | | | | | Reserved | x | x | x | x | x | x | x | x | xx | |
| | 13 | 8014 | 1 | Encoding | Bit encoding | Unspecified | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | | | | | NRZ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| | | | | | | FEC | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 | |
| | 14 | 8015 | 2 | Bit Rate | Nominal Bit Rate in multiples of 1Mb/s | Reserved | x | x | x | x | x | x | x | x | xx | |
| | | | | | | Unspecified | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | | | | | x | x | x | x | x | x | x | x | xx | | |
| | 16 | 8017 | 1 | Protocol | Protocol Type | Unspecified | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | | | | | 10GbE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| | | | | | | 10GFC | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 | |
| | | | | | | WIS | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4 | |
| | | | | | | LSS | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 8 | |
| | | | | | | SONET/SDH | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | |
| | | | | | | Reserved | x | x | x | x | x | x | x | x | xx | |
| | | | | | | Unspecified | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | | | | | 10GBASE-SR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| | | | | | | 10GBASE-LR | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 | |
| | 17 | 8018 | 10 | Standards Compliance Codes | 10GbE Code Byte 0 | 10GBASE-ER | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4 | |
| | | | | | | 10GBASE-LX4 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 8 | |
| | | | | | | 10GBASE-SW | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | |
| 10GBASE-LW4 | | | | | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 | | |
| 10GBASE-LW | | | | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40 | | |
| 10GBASE-EW | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 | | |
| Reserved | | | | | | x | x | x | x | x | x | x | x | xx | | |
| 10GbE Code Byte 1 | | | | | | | | | | | | | | | | |

NVR Register Map (continued)

| | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----|------|----|----------------------------|-----------------------|-----------------------|-------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|----|
| Basic | 17 | 8018 | 10 | Standards Compliance Codes | SONET/SDH Code Byte 0 | Unspecified | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | |
| | | | | | | S-64.1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | | | | | | S-64.2a | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 2 |
| | | | | | | S-64.2b | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4 |
| | | | | | | S-64.3a | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 |
| | | | | | | S-64.3b | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 10 |
| | | | | | | S-64.5a | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 20 |
| | | | | | | S-64.5b | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 40 |
| | | | | | | Reserved | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 |
| | | | | | | SONET/SDH Code Byte 1 | Unspecified | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | I-64.1r | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| | | | | | I-64.1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 2 | |
| | | | | | I-64.2r | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | |
| | | | | | I-64.2 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | |
| | | | | | I-64.3 | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 10 | |
| | | | | | I-64.5 | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 20 | |
| | | | | | Reserved | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 40 | |
| | | | | | Reserved | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 | |
| | | | | | SONET/SDH Code Byte 2 | | Unspecified | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | L-64.1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | |
| | | | | | | L-64.2a | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 2 | |
| | | | | | | L-64.2b | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | |
| | | | | | | L-64.2c | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | |
| | | | | | | L-64.3 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 10 | |
| | | | | | | Reserved | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 20 | |
| | | | | | | Reserved | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 40 | |
| | | | | | | Reserved | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 | |
| | | | | | | SONET/SDH Code Byte 3 | Unspecified | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | V-64.2a | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | |
| | | | | | V-64.2b | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 2 | |
| | | | | | V-64.3 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | |
| | | | | | Reserved | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | |
| | | | | | Reserved | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 10 | |
| | | | | | Reserved | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 20 | |
| | | | | | Reserved | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 40 | |
| | | | | | Reserved | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 | |
| | | | | | 10GFC Code Byte 0 | | Reserved | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | xx |
| | | | | | 10GFC Code Byte 1 | Reserved | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | xx | |
| | | | | | 10GFC Code Byte 2 | Reserved | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | xx | |
| | | | | | 10GFC Code Byte 3 | Reserved | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | xx | |

NVR Register Map (continued)

| | | | | | | | | | | | | | | | | | |
|-----------------|-------------------|-----------------|------------|--|---|---------------|---|---|---|---|---|----|---|----|----|----|---|
| Basic | 27 | 8022 | 2 | Range | Specifies transmission range in 10 m increments | | x | x | x | x | x | x | x | x | x | xx | |
| | 29 | 8024 | 2 | Fibre Type | Fibre Type Byte 0 | Unspecified | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | MM, generic | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| | | | | | | 50/125 only | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | |
| | | | | | | 62.5/125 only | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4 | |
| | | | | | | POF | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 8 | |
| | | | | | | HPCF | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 10 | |
| | | | | | | SM, generic | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 20 | |
| | | | | | | NDSF only | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 40 | |
| | | | | | | NZDSF only | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 | |
| | | | | | | Unspecified | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | Fibre Type Byte 1 | Large core only | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | | | | | |
| | | PMF only | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 | | | | | |
| | | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4 | | | | | |
| | | Reserved | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 8 | | | | | |
| | | Reserved | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 10 | | | | | |
| | | Reserved | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 20 | | | | | |
| | | Reserved | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 40 | | | | | |
| | | Reserved | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 | | | | | |
| | 31 | 8026 | 3 | Wavelength | Centre Optical Wavelength in 0.01nm increments | | x | x | x | x | x | x | x | x | xx | | |
| | 34 | 8029 | 4 | Vendor OUI | Transceiver Vendor OUI | | x | x | x | x | x | x | x | x | xx | | |
| | 38 | 802D | 16 | Vendor Name | Transceiver vendor name in ASCII | | x | x | x | x | x | x | x | x | xx | | |
| | 54 | 803D | 16 | Vendor PN | Part number provided by transceiver vendor in ASCII | | x | x | x | x | x | x | x | x | xx | | |
| 70 | 804D | 4 | Vendor Rev | Revision level for part number provided by vendor ASCII | | x | x | x | x | x | x | x | x | xx | | | |
| 74 | 8051 | 2 | Options | Indicates which optional transceiver signals are implemented | | x | x | x | x | x | x | x | x | xx | | | |
| 76 | 8053 | 16 | Vendor SN | Vendor serial number in ASCII | | x | x | x | x | x | x | x | x | xx | | | |
| 92 | 8063 | 4 | Date Code | Vendor manufacturing date code in ASCII | Year | x | x | x | x | x | x | x | x | x | xx | | |
| 96 | 8067 | 2 | | | Month | x | x | x | x | x | x | x | x | x | xx | | |
| 98 | 8069 | 2 | | | Day | x | x | x | x | x | x | x | x | x | xx | | |
| 100 | 806B | 2 | | | Lot code | x | x | x | x | x | x | x | x | x | x | xx | |
| 102 | 806D | 1 | | | | x | x | x | x | x | x | x | x | x | xx | | |
| Customer | 103 | 806E | 64 | Customer Area | Customer Writeable Area | | x | x | x | x | x | x | x | x | xx | | |
| Vendor | 167 | 80AE | 89 | Vendor Specific | Vendor Specific | | x | x | x | x | x | x | x | x | xx | | |
| Extended Vendor | 256 | 8107 | n-256 | Extended Vendor | Extended Vendor Specific | | x | x | x | x | x | x | x | x | xx | | |

20.10 Link Alarm Status Interrupt (LASI)

20.10.1 Overview

The link alarm status interrupt (LASI) is an active-low output (pin 9) from the XENPAK module that, when asserted, indicates a link fault condition. Control registers are provided so that LASI may be programmed to assert only for specific fault conditions. A set of status registers are also provided to allow interrupt service routines to identify the source of the fault with a minimal number of register reads.

When XENPAK diagnostics are included, the LASI function can incorporate diagnostic-based alarms to increase its fault isolation capabilities.

20.10.2 Operation

A top-level block diagram of LASI is shown in Fig 23

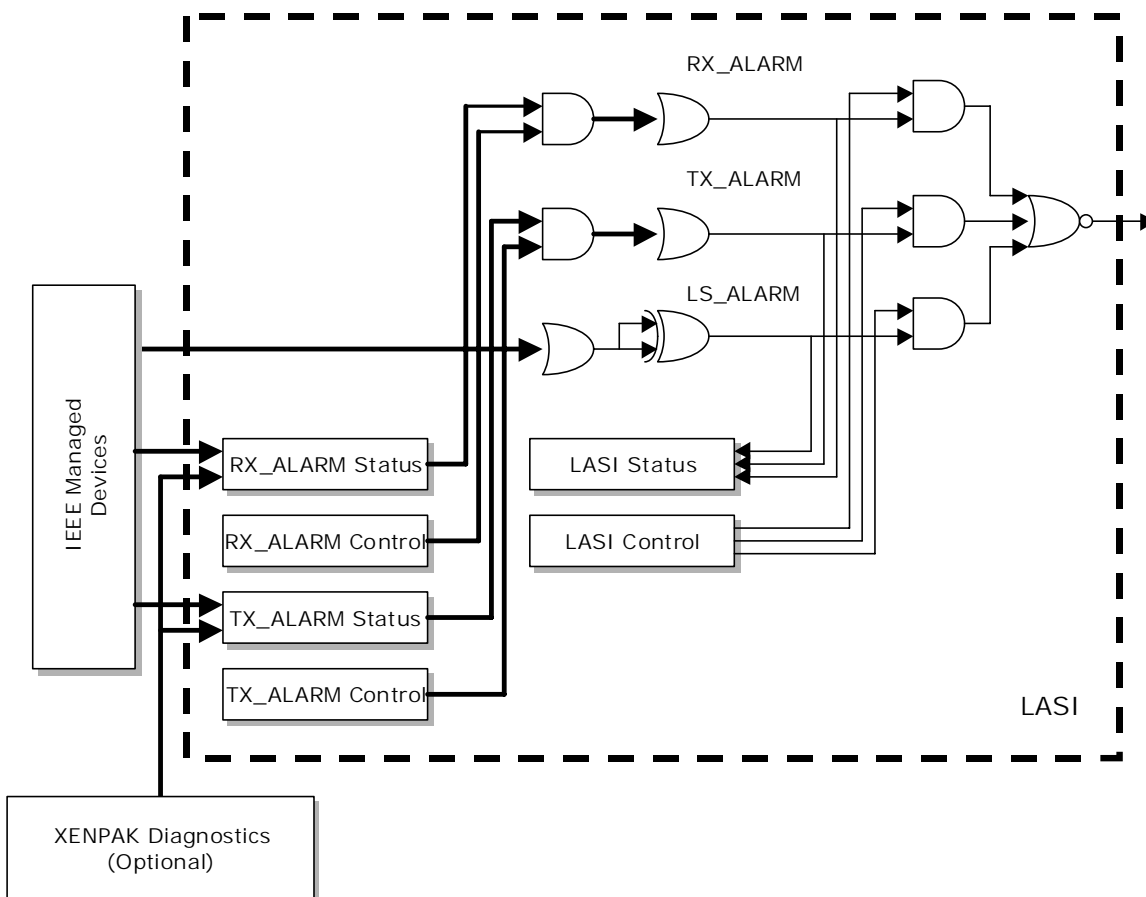


Fig 23. LASI Block Diagram

20.10.3 RX_ALARM Status

Assertion of RX_ALARM indicates that a fault has occurred in the receive path of the XENPAK module. RX_ALARM shall be the logic OR of the bits in register 0x9003.

The contents of the RX_ALARM status register are shown in Table x. Several bits in this register are linked to latch-high, clear on read bits in the IEEE standard register space (i.e. local fault bits). A read to either bit shall have the effect of clearing the status indicator in both locations.

For example, a PHY XS Receive Local Fault will cause both bit 4.8.10 and bit 0 of the RX_ALARM status register to latch high. A read to register 4.8 clears both 4.8.10 and bit 0 of the RX_ALARM status register. Similarly, a read to the RX_ALARM status register clears bit 0 and bit 4.8.10.

Table 17 RX_ALARM Status Register (0x9003)

| Bit | Description | Properties ¹ |
|-------|---|-------------------------|
| 15:11 | Reserved (set to zero) | RO |
| 10 | Vendor Specific | — |
| 9 | WIS Local Fault (bit 2.1.7) | O/RO/LH |
| 8:6 | Vendor Specific | — |
| 5 | Receive Optical Power Fault | O/RO/LH |
| 4 | PMA/PMD Receiver Local Fault (bit 1.8.10) | O/RO/LH |
| 3 | PCS Receive Local Fault (bit 3.8.10) | RO/LH |
| 2:1 | Vendor Specific | — |
| 0 | PHY XS Receive Local Fault (bit 4.8.10) | RO/LH |

1 O = optional, RW = read/write, RO = read only, LH = latch high, clear on read (note that if the condition exists following register read, the bit will not be cleared).

20.10.4 RX_ALARM Control

RX_ALARM may be programmed to assert only when specific receive path fault condition(s) are present. The programming is performed by setting the contents of a mask register located at offset 0x9000. The contents of register 0x9003 shall be AND'd with the contents of register 0x9000 prior to application of the OR function that generates the RX_ALARM signal.

Table 18 RX_ALARM Control Register (0x9000)

| Bit | Description | Properties ¹ |
|-------|-------------------------------------|-------------------------|
| 15:11 | Reserved (set to zero) | RO |
| 10 | Vendor Specific | RW |
| 9 | WIS Local Fault Enable | Note 2 |
| 8:6 | Vendor Specific | RW |
| 5 | Receive Optical Power Fault Enable | Note 2 |
| 4 | PMA/PMD Receiver Local Fault Enable | Note 2 |
| 3 | PCS Receive Local Fault Enable | RW |
| 2:1 | Vendor Specific | RW |
| 0 | PHY XS Receive Local Fault Enable | RW |

1. O = optional, RW = read/write, RO = read only, LH = latch high, clear on read (note that if the condition exists following register read, the bit will not be cleared).
 2. Optional features that are unsupported shall have their enable bit forced to zero.

20.10.5 TX_ALARM Status

Assertion of TX_ALARM indicates that a fault has occurred in the transmit path of the XENPAK module. TX_ALARM shall be the logic OR of the bits in register 0x9004.

The contents of the TX_ALARM status register are shown in Table x. Several bits in this register are linked to latch-high, clear on read bits in the IEEE standard register space (i.e. local fault bits). A read to either bit shall have the effect of clearing the status indicator in both locations (refer to 20.10.3 for an example).

Table 19 TX_ALARM Status Register (0x9004)

| Bit | Description | Properties |
|-------|--|------------|
| 15:11 | Reserved (set to zero) | RO |
| 10 | Vendor Specific | — |
| 9 | Laser Bias Current Fault | O/RO/LH |
| 8 | Laser Temperature Fault | O/RO/LH |
| 7 | Laser Output Power Fault | O/RO/LH |
| 6 | Transmitter Fault | RO/LH |
| 5 | Vendor Specific | — |
| 4 | PMA/PMD Transmitter Local Fault (1.8.11) | O/RO/LH |
| 3 | PCS Transmit Local Fault (3.8.11) | RO/LH |
| 2:1 | Vendor Specific | — |
| 0 | PHY XS Transmit Local Fault (4.8.11) | RO/LH |

1. O = optional, RW = read/write, RO = read only, LH = latch high, clear on read (note that if the condition exists following register read, the bit will not be cleared).

20.10.6 TX_ALARM Control

TX_ALARM may be programmed to assert only when specific transmit path fault condition(s) are present. The programming is performed by setting the contents of a mask register located at offset 0x9001. The contents of register 0x9004 shall be AND'd with the contents of register 0x9001 prior to application of the OR function that generates the TX_ALARM signal.

Table 20 TX_ALARM Control Register (0x9001)

| Bit | Description | Properties |
|-------|--|------------|
| 15:11 | Reserved (set to zero) | RO |
| 10 | Vendor Specific | RW |
| 9 | Laser Bias Current Fault Enable | Note 2 |
| 8 | Laser Temperature Fault Enable | Note 2 |
| 7 | Laser Output Power Fault Enable | Note 2 |
| 6 | Transmitter Fault Enable | RW |
| 5 | Vendor Specific | RW |
| 4 | PMA/PMD Transmitter Local Fault Enable | Note 2 |
| 3 | PCS Transmit Local Fault Enable | RW |
| 2:1 | Vendor Specific | RW |
| 0 | PHY XS Transmit Local Fault Enable | RW |

1. O = optional, RW = read/write, RO = read only, LH = latch high, clear on read (note that if the condition exists following register read, the bit will not be cleared).
2. Optional features that are unsupported shall have their enable bit forced to zero.

20.10.7 LS_ALARM

The LS_ALARM shall be asserted each time Link Status, defined in 20.10.8, changes state. This feature eliminates the need to periodically poll a module for status. A fault condition will assert TX_ALARM, RX_ALARM, and set Link Status to FALSE. TX_ALARM and RX_ALARM may be masked to prevent persistent interrupt. When the fault condition is removed, Link Status will change state to TRUE causing the

assertion of the LS_ALARM. The interrupt service routine may then remove the mask on TX_ALARM and RX_ALARM to resume normal monitoring.

20.10.8 Link Status Definition

Link Status is a real-time indicator of link health generated internally by LASI for use in the LS_ALARM interrupt definition. Link Status shall be the logic OR of the signals shown in Table 21

Table 21 Link Status Input Signals

| Signal | Source |
|-----------------------------|---------|
| Global PMD Signal OK | 1.10.0 |
| PCS Block Lock ¹ | 3.32.0 |
| PHY XS Lane Alignment | 4.24.12 |

1. In the case of the 10GBASE-LX4 PCS, the Lane Alignment status bit (3.24.12) may be used rather than Block Lock.

Additional signals may be included in the Link Status definition but this is beyond the scope of this MSA. Inputs to Link Status shall not be latched signals.

20.10.9 LASI Status

Register 0x9005 contains a top-level of the cause of the interrupt. The contents of this register are given in Table 22.

Table 22 LASI Status Register (0x9005)

| Bit | Description | Properties ¹ |
|------|-----------------|-------------------------|
| 15:8 | Reserved | RO |
| 7:3 | Vendor Specific | — |
| 2 | RX_ALARM | RO |
| 1 | TX_ALARM | RO |
| 0 | LS_ALARM | RO/LH |

1. O = optional, RW = read/write, RO = read only, LH = latch high, clear on read (note that if the condition exists following register read, the bit will not be cleared).

Note that the RX_ALARM and TX_ALARM indications are the logic OR of the contents of registers 0x9003 and 0x9004 respectively. Therefore, these alarms will persist until the bit(s) reflecting the source of interrupt are cleared.

20.10.10 LASI Control

Register 0x9002 is a LASI control register that allows global masking of the RX_ALARM, TX_ALARM, and LS_ALARM inputs. The contents of this register are given in Table 23

Table 23 LASI Control Register (0x9002)

| Bit | Description | Properties ¹ |
|------|-----------------|-------------------------|
| 15:8 | Reserved | RO |
| 7:3 | Vendor Specific | RW |
| 2 | RX_ALARM Enable | RW |
| 1 | TX_ALARM Enable | RW |
| 0 | LS_ALARM Enable | RW |

1. O = optional, RW = read/write, RO = read only, LH = latch high, clear on read (note that if the condition exists following register read, the bit will not be cleared).

20.10.11 LASI Timing Requirements

LASI shall be asserted within 10 ms following the detection of a fault condition. LASI shall be cleared within 10 ms of the register read operation that clears the fault indicator.

20.10.12 Relationship between LASI and XENPAK Diagnostics

Receive optical power, laser output power, laser bias current, and laser temperature fault indications are optional inputs to the LASI function which are also covered by the XENPAK diagnostics. While this fault indications have a vendor specific definition, it is recommended that when XENPAK diagnostics are implemented, these fault indications are the logic OR of high/low alarms for the parameter of interest. For example, Receive Optical Power Fault would be the logic OR of the Receive Optical Power High and Receive Optical Power Low alarms from the XENPAK diagnostics.

When implemented according to this definition, an additional register reads will be required to clear a diagnostic related interrupt. Since LASI fault indications are recommended to be the logic OR of latched diagnostics alarms, the interrupt cannot be cleared until the diagnostic alarm register is read. These additional register reads will not only clear the interrupt but also indicate whether the fault occurred due to high or low parameter levels.

20.11 XENPAK Diagnostics

20.11.1 Overview

PMD analogue signals are optional. They are monitored, converted and digitally reported through MDIO registers by a XENPAK transceiver.

The signals to be monitored are:

- Laser Temperature
- Laser Bias
- TX Output Power
- Received Power

The converted signals should to fit into a standard data format, TBD.

Four identical sets of results registers are provided to accommodate multi-channel implementations of XENPAK, for example, WDM and parallel optics. Result register 0 is the default register for serial PMDs.